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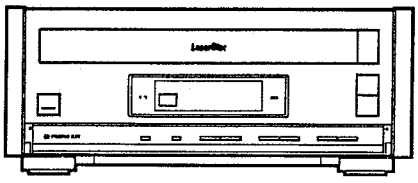
The future of sound and vision.

Service Manual



ORDER NO.
ARP2093

LD PLAYER

LD-S2

• This manual is applicable to the KU/CA type.

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This service manual is intended for qualified service technicians; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.
Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING
Lead in solder used in this product is listed by the California Health and Welfare agency as a known reproductive toxicant which may cause birth defects or other reproductive harm (California Health & Safety Code, Section 25249.5).
When servicing or handling circuit boards and other components which contain lead in in solder, avoid unprotected skin contact with the solder. Also, when soldering do not inhale any smoke or fumes produced.

1. SAFETY INFORMATION

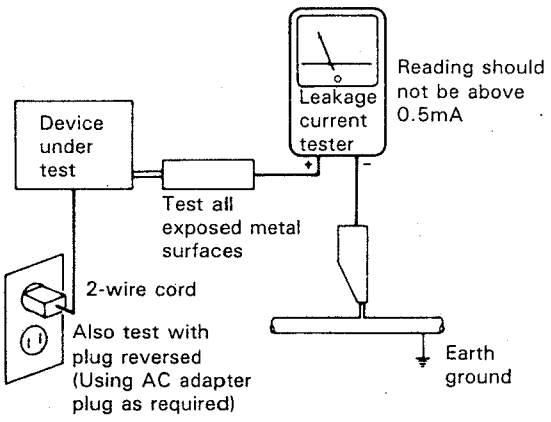
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.



AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

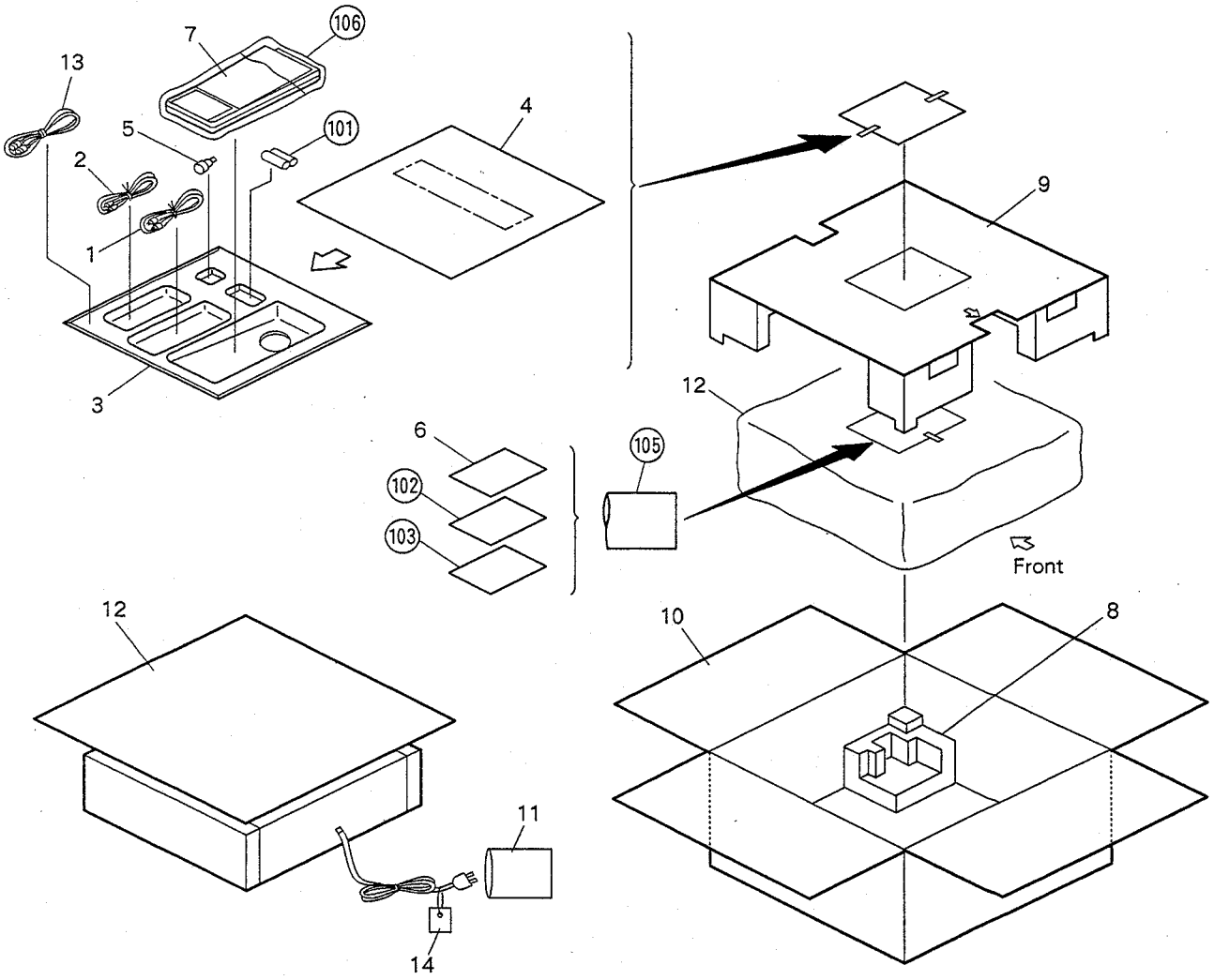
Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.
The use of a substitute replacement component which dose not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

2. PACKING

Parts List

Mark	No.	Part No.	Description
	1	PDE1003	Cord with pin plug
	2	VDE1003	Video cable
	3	VHX1017	Parts case (A)
	4	VHX1014	Parts case (B)
	5	VKX1004	BNC-pin conversion plug
	6	VRB1028	Operating instructions (English)
	7	VXX1370	Remote control unit
	8	VHA1051	Pad (A)
	9	VHA1052	Pad (B)
	10	VHG1092	Packing case
	11	VHL1004	Mirror mat bag
	12	VHL1014	Mirror mat bag
	13	VED1013	S video cable
	14	VRW1146	Caution tag
	101		Battery (SUM-3)
	102		Caution card
	103		Caution card (UC)
	104		• • • • •
	105		Polyethylene bag
	106		Polyethylene bag



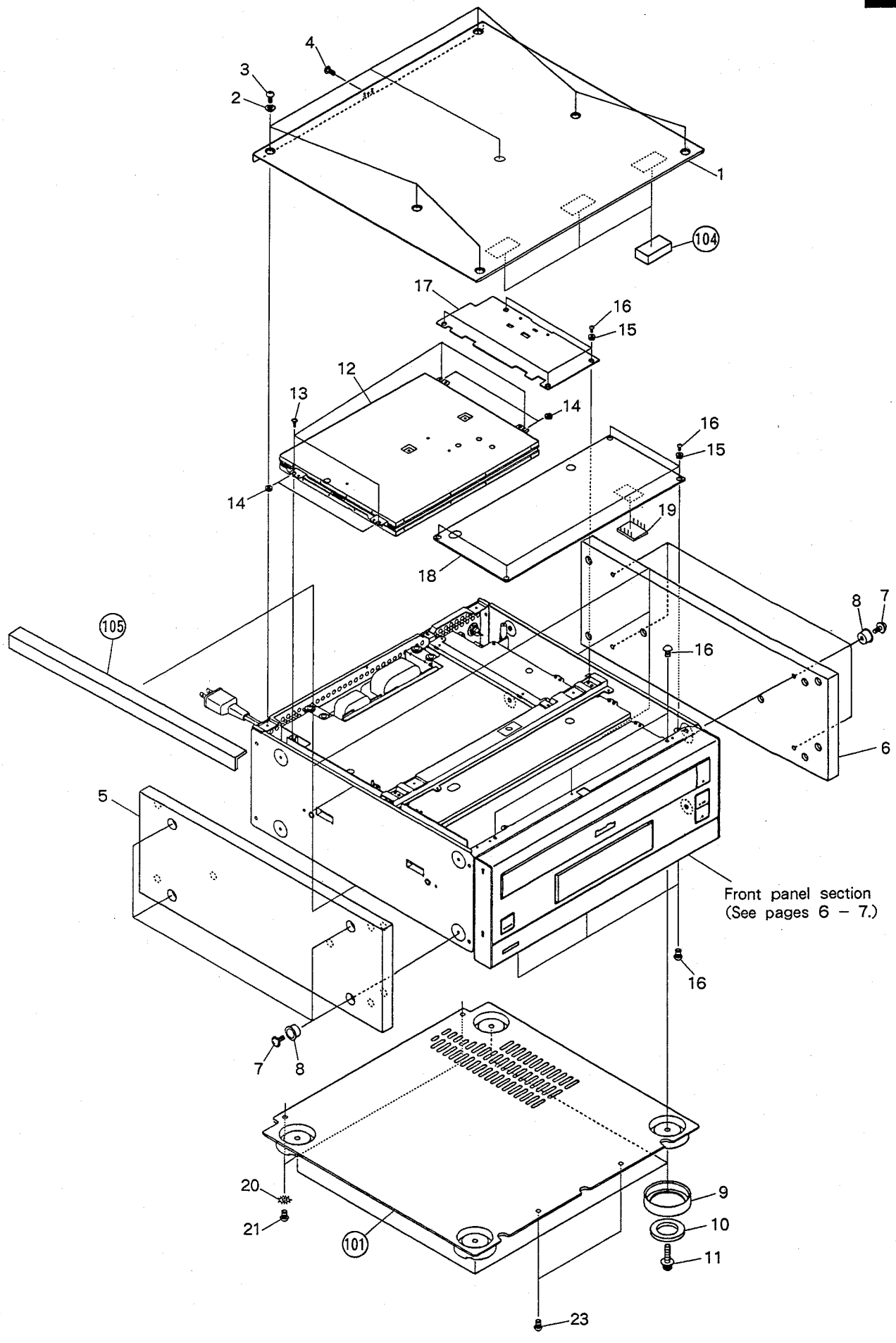
3. EXPLODED VIEWS AND PARTS LIST

NOTES :
- Parts without part number cannot be supplied.
- The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
- Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.

3.1 EXTERIOR SECTION

Parts List of Exterior Section

Mark	No.	Part No.	Description
	1	VNA1102	Top panel
	2	PLA1029	Top plate collar
	3	BBT30P080FBR	Screw
	4	BBT30P060FBR	Screw
	5	VAP1009	Side wood (L)
	6	VAP1010	Side wood (R)
	7	VBA1020	Ornament screw (B)
	8	PNW1238	Wood collar
	9	VNK1408	Ornament cap
	10	VEC1289	Cushion
	11	VBA1004	Screw
◉	12	VWS1077	VSMB assembly
	13	PBA1014	Screw (B)
	14	VEB1112	Rubber bushing (B)
	15	VEB1113	Rubber bushing (C)
	16	ABZ30P080FCC	Screw
◉	17	VWV1093	VTRB assembly
◉	18	VWG1082	CONT assembly
	19	VYW1467	Program P ROM-S (IC102)
	20	WG40FCU	Washer
	21	IBZ30P100FCC	Screw
	22	BCZ30P080FCC	Screw
	23	ECT40P080FZK	Screw
	101		Bottom plate
	102		• • • • •
	103		• • • • •
	104		Cushion
	105		Dump cushion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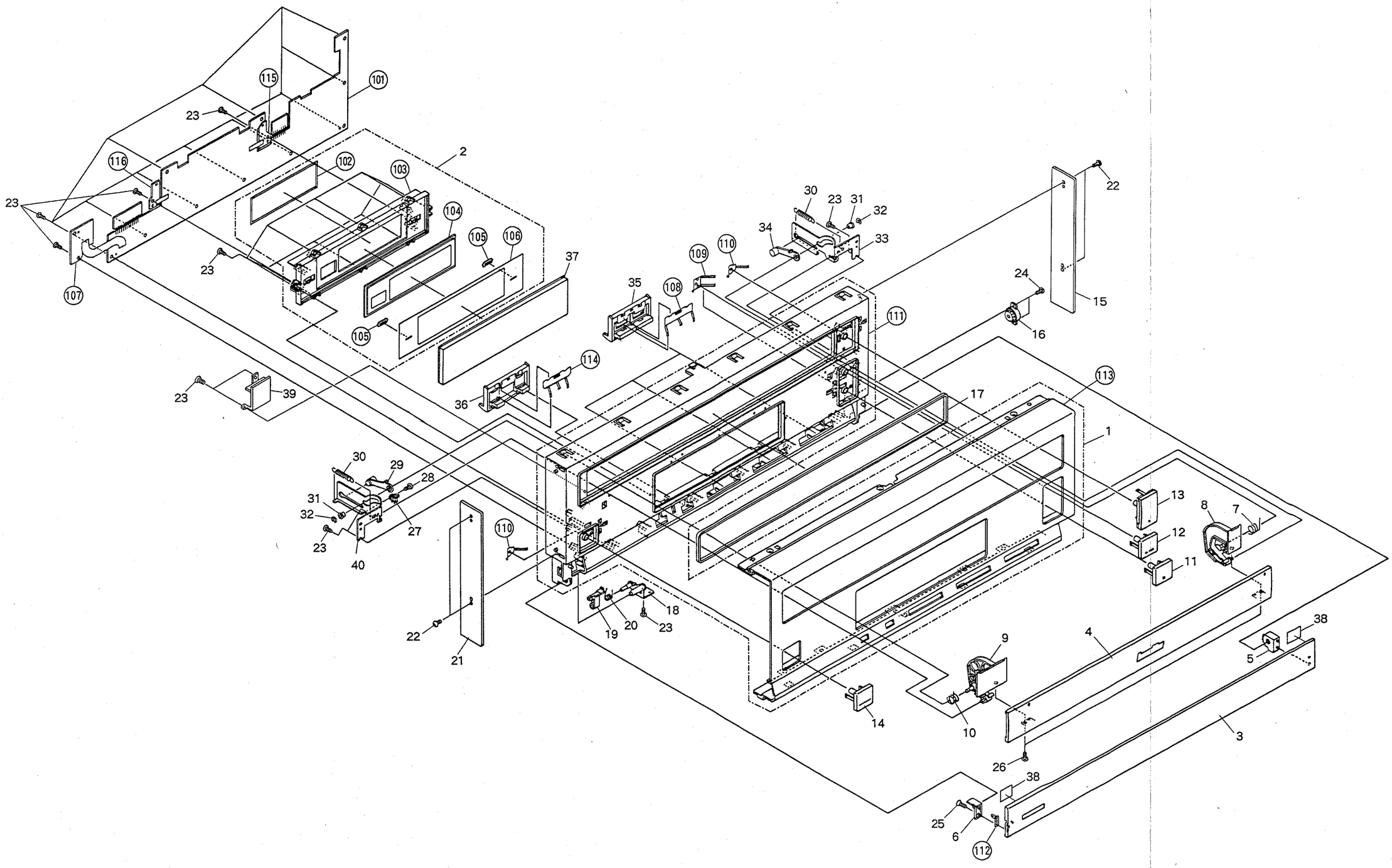
Front panel section
(See pages 6 – 7.)

3.2 FRONT PANEL SECTION

Parts List of Front Panel Section

Mark	No.	Part No.	Description
	1	VXX1382	Front panel assembly-S
	2	VXX1404	Display assembly-S
	3	VXA1446	Pocket alum. assembly
	4	VXA1461	Door alum. assembly
	5	VNL1295	Pocket arm (R)
	6	VNL1294	Pocket arm (L)
	7	VBH1119	Door arm spring (R)
	8	VXA1378	Door arm (R) assembly
	9	VXA1377	Door arm (L) assembly
	10	VBH1118	Door arm spring (L)
	11	VXA1373	Stop button assembly
	12	VXA1372	Play button assembly
	13	VXA1374	Open button assembly
	14	VXA1371	Power button assembly
	15	VAH1120	Gold panel (R)
	16	REC1013	Dumper assembly
	17	VEB1126	High pack rubber
	18	VXA1379	Pocket holder assembly
	19	VNL1263	Pocket lock
	20	VBH1120	Pocket spring
	21	VAH1119	Gold panel (L)
	22	BPZ30P080FCU	Screw
	23	BPZ26P060FCU	Screw
	24	BPZ20P060FCU	Screw
	25	CMZ26P040FZK	Screw
	26	CPZ26P060FCU	Screw
	27	VSK1010	Slide switch (S3) (DOOR)
	28	PMZ20P060FCU	Screw
	29	VXA1380	Arm joint (L) assembly
	30	VBH1106	Door spring
	31	VLL1267	Joint roller
	32	YE20FUC	Washer
	33	VNE1392	Arm base (R)
	34	VXA1381	Arm joint (R) assembly
	35	VXA1375	Pocket button (A) assembly
	36	VXA1376	Pocket button (B) assembly
	37	VNK1379	Acrylic panel
	38	VEC1324	Pocket cushion
	39	VNK1422	Sub panel
	40	VNE1391	Arm base (L)
	41	VNE1498	Arm plate
	42	AAM1001	Name plate

Mark	No.	Part No.	Description
	101		KEYB assembly
	102		FL filter
	103		Display base
	104		FL panel
	105		LED lens
	106		Display plate
	107		PWSB assembly
	108		Earth plate (B)
	109		Earth plate (C)
	110		Earth plate (D)
	111		Front panel
	112		Earth plate (E)
	113		Front alum.
	114		Earth plate (A)
	115		LEDA assembly
	116		LEDB assembly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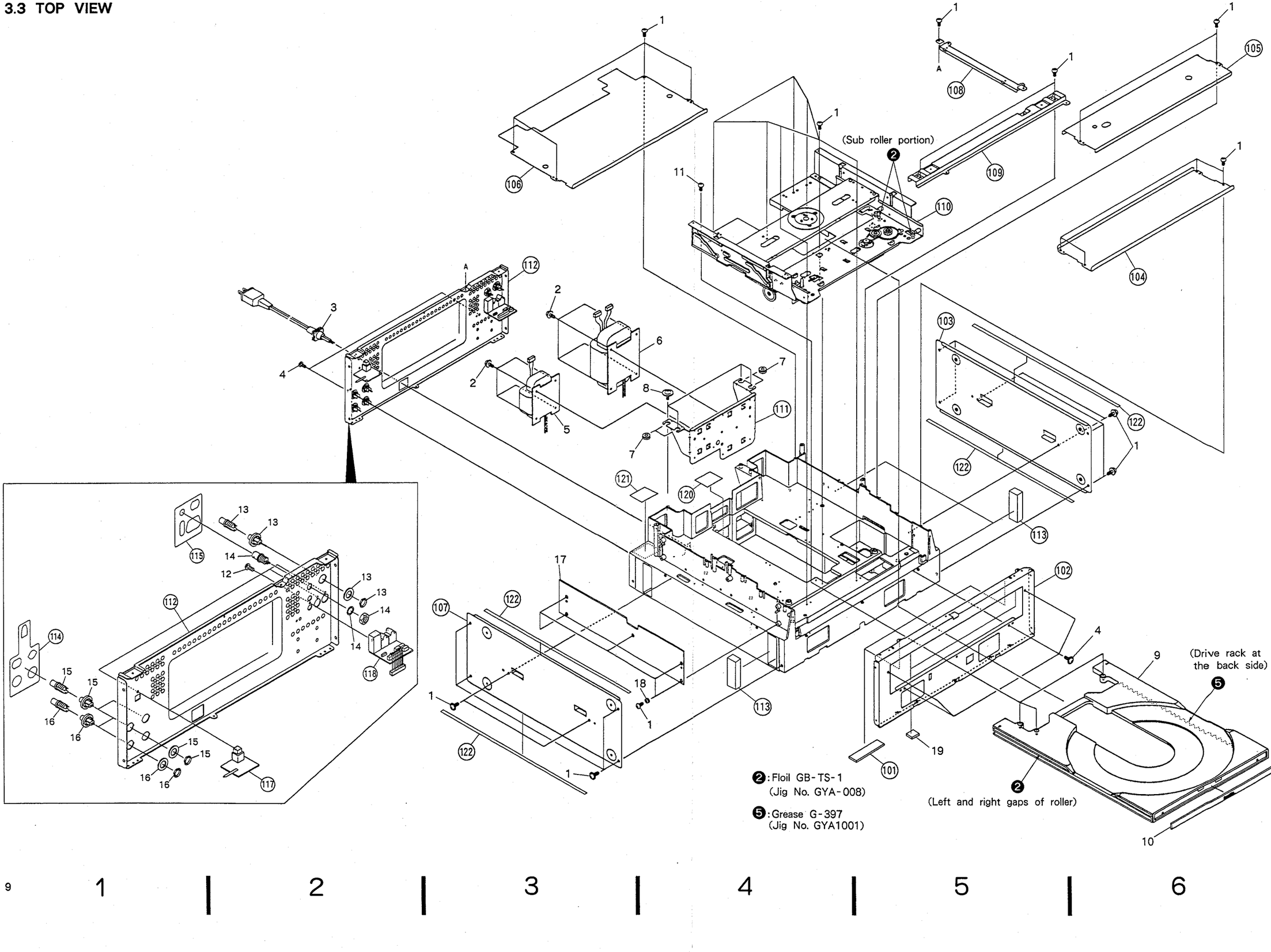
3.3 TOP VIEW


(Sub roller portion)
❷:Floil GB-TS-1
(Jig No. GYA-008)
❺:Grease G-397
(Jig No. GYA1001)
(Left and right gaps of roller)
(Drive rack at the back side)

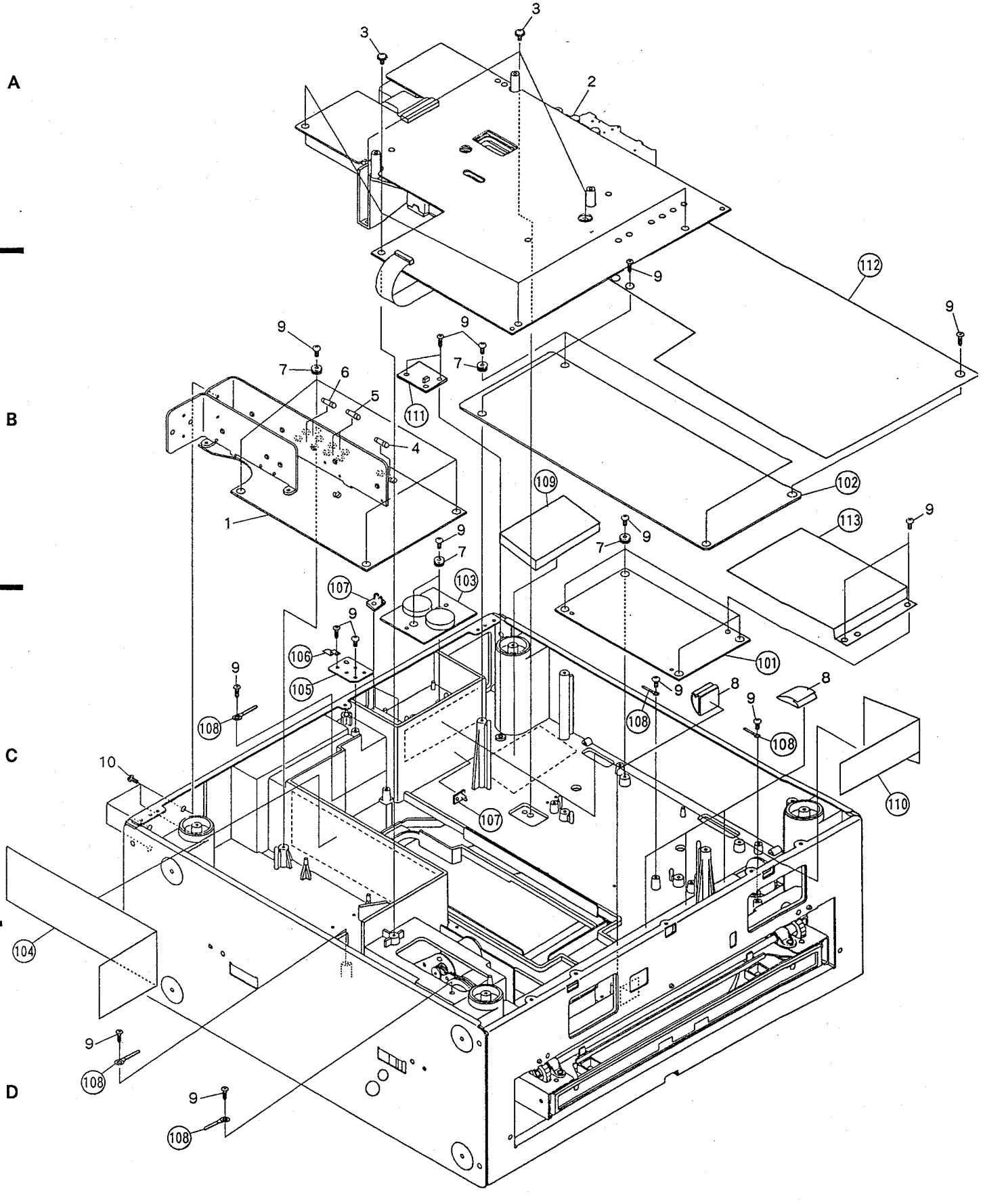
Parts List of Top View

Mark	No.	Part No.	Description
	1	ABZ30P080FCC	Screw
	2	ABZ30P050FCC	Screw
⚠	3	VDG1041	AC power cord
	4	IBZ30P080FBR	Screw
⚠	5	VTT1076	Power transformer (AUDIO)
⚠	6	VTT1075	Power transformer (MAIN)
	7	VEB1111	Rubber bushing (A)
	8	VBA1003	Screw
	9	VNK1466	Carry
	10	VNK1393	Carry escutheon
	11	BPZ30P120FCU	Screw
	12	BPZ30P080FBR	Screw
	13	VKB1024	1P pin jack (Body, washer and nut)
	14	VKB1017	BNC connector (Body, washer and nut)
	15	PKB1012	1P pin jack L (Body, washer and nut)
	16	PKB1013	1P pin jack R (Body, washer and nut)
◉	17	VWV1112	DCDR assembly
	18	VEB1113	Rubber bushing (C)
	19	VEC1331	Cushion (L)
	101		Cushion (B)
	102		Panel holder
	103		Side cover (R)
	104		Loading cover (F)
	105		Loading cover (M)
	106		Loading cover (R)
	107		Side cover (L)
	108		Reinforcement bridge (B)
	109		Reinforcement bridge (A)
	110		Loading assembly
	111		Transformer base
	112		Rear panel
	113		Cushion (A)
	114		Label (R)
	115		Label (L)
	116		Earth plate
	117		DOUT assembly
	118		VOUT assembly
	119		• • • • •
	120		Shield sheet (D)
	121		Shield sheet (E)
	122		Dump cushion (B)

3.4 BOTTOM VIEW

Parts List of Bottom View

Mark	No.	Part No.	Description
◉	1	VWR1034	SYPS assembly
◉	2	VWS1062	SRVD assembly
	3	PMB30P060FCU	Screw
⚠	4	REK-080	Fuse (1A) (FU5)
⚠	5	REK-084	Fuse (4A) (FU1, 2)
⚠	6	VEK-018	Fuse (3A) (FU3, 4)
	7	VEB1113	Rubber bushing (C)
	8	VEC1323	Shell clip
	9	ABZ30P080FCC	Screw
	10	IBZ30P080FBR	Screw
	101		FMDB assembly
	102		DACB assembly
	103		LSFB assembly
	104		Shield sheet (B)
	105		Earth plate
	106		Earth plate
	107		Mini clamp
	108		Cord holder
	109		Capacitor cushion
	110		Shield sheet (C)
	111		SETB assembly
	112		Shield sheet (F)
	113		Shield sheet (A)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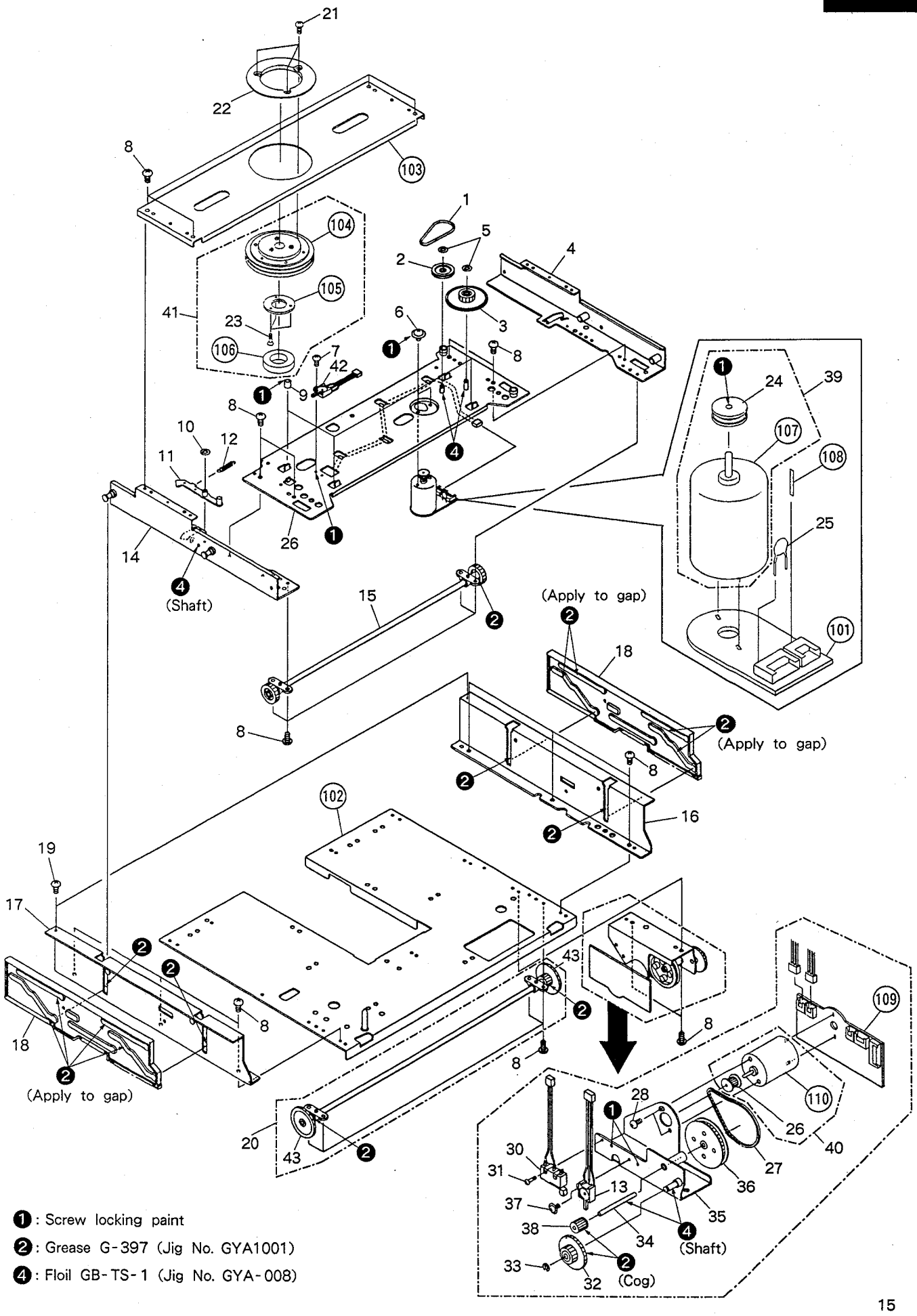
3.5 CLAMPER AND LOADING ASSEMBLY SECTION

Parts List of Clamper and Loading Assembly Section

Mark	No.	Part No.	Description
	1	VEB1110	Loading belt
	2	VNL1287	Pulley (A)
	3	VNL-496	Gear (B) (for Horizontal)
	4	VXA1442	Roller plate (R) assembly
	5	WT34D060D050	Washer
	6	BMZ30P030FCU	Screw
	7	BMZ26P050FCU	Screw
	8	BBZ30P060FCC	Screw
	9	VEB1087	Rubber tube
	10	WT21D040D050	Washer
	11	VXA1397	Lock lever assembly
	12	VBH1115	Lock spring
	13	VSK1013	Lever switch (S1) (V UP/DOWN)
	14	VXA1443	Roller plate (L) assembly
	15	VXA1400	Synchro gear (B) assembly
	16	VXA1391	Guide (R) assembly
	17	VXA1392	Guide (L) assembly
	18	VNL1269	Rack
	19	BCZ30P080FCC	Screw
	20	VXA1399	Synchro gear (A) assembly
	21	BPZ26P060FCU	Screw
	22	VNL1130	Clamper head
	23	CPZ20P060FMC	Screw
	24	VLL1240	Pulley (B)
	25	CGDYX473M25	Ceramic capacitor (C6)
	26	VNL1051	Motor pulley
	27	VEB1038	Synchro belt
	28	BMZ30P030FCU	Screw
	29		• • • • •
	30	VSF1001	Micro switch (S4) (V MID)
	31	AMZ20P080FCU	Screw
	32	VNL-496	Gear (B) (for Vertical)
	33	WT34D060D050	Washer
	34	VLL1237	Gear (A) shaft
	35	VXA1388	M holder assembly
	36	VXA-477	Pulley (L) assembly
	37	BMZ26P050FCU	Screw
	38	VNL1020	Gear (A)
	39	VXX1353	Loading motor (H) assembly
	40	VXX1352	Loading motor (V) assembly
	41	VXX1354	Clamper assembly-S
	42	VSK1013	Lever switch (S2) (H IN/OUT)
	43	VNL-497	Synchro gear
	101		LODH assembly
	102		Sub chassis assembly
	103		Clamper holder
	104		Clamper assembly
	105		Yoke plate
	106		Magnet
	107		Power motor
	108		PCB binder
	109		LODV assembly
	110		Power motor

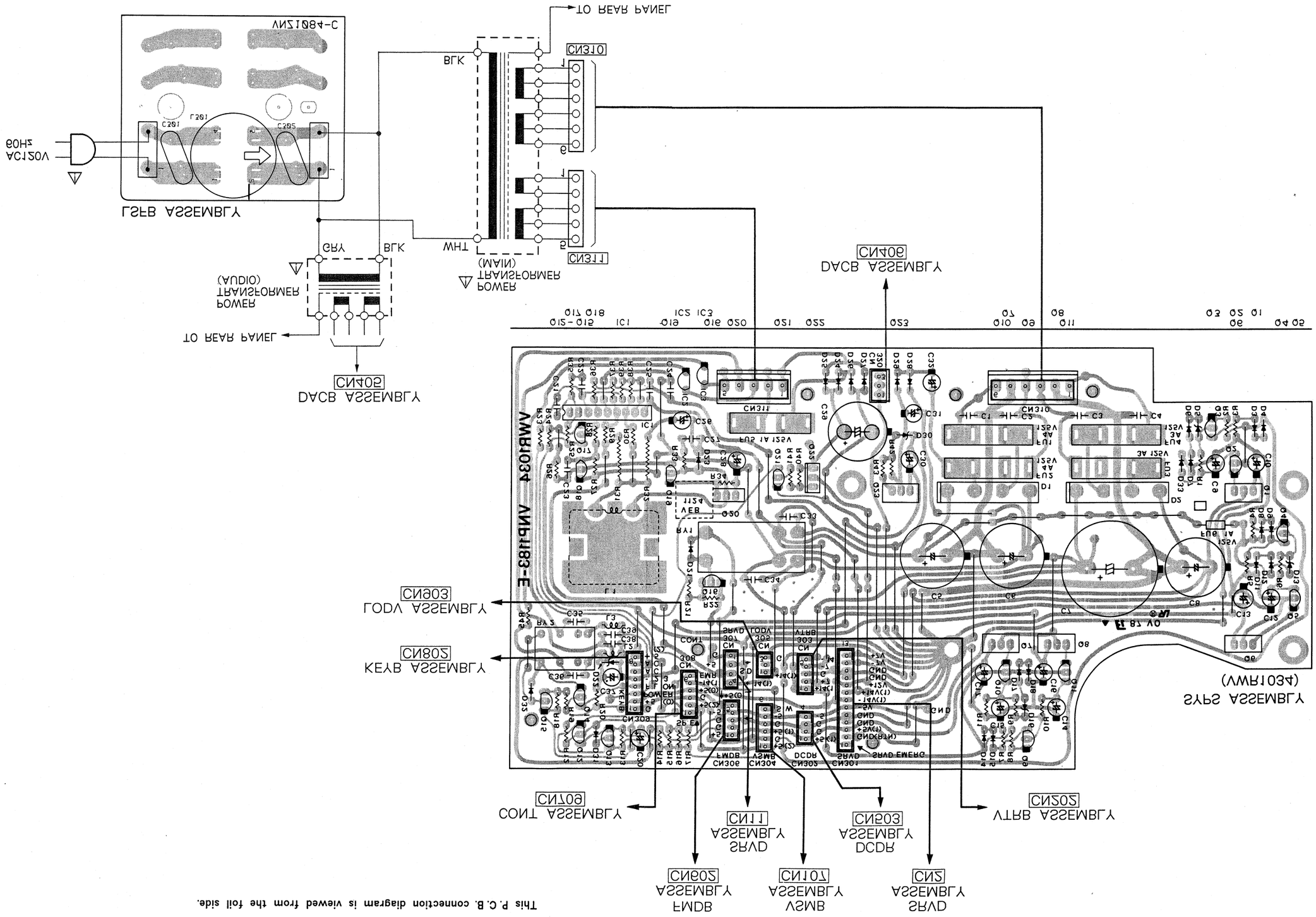

(Shaft)
(Apply to gap)
(Apply to gap)
(Apply to gap)
(Shaft)
(Cog)
❶ : Screw locking paint
❷ : Grease G-397 (Jig No. GYA1001)
❹ : Floil GB-TS-1 (Jig No. GYA-008)

3.6 MECHANISM BASE ASSEMBLY

Parts List of Mechanism Base Assembly

Mark	No.	Part No.	Description
	1	DXP1005	Drive unit
	2	DNS1051	Shaft holder
	3	VXP1003	Speed detection unit
	4	DLA1172	D shaft
	5	DLA1173	S shaft
	6	VBH1121	Lock spring
	7	PMB30P060FCU	Screw
	8	IBZ30P080FCC	Screw
	9	VEB1128	Stopper
	10	VBH1108	HT spring
	11	VBH1109	Fixed spring
	12	SMZ26H120FZK	Screw
	13	DBA1013	Adjustment screw
	14	VXA1393	Adjustment plate assembly
	15	VXA1394	Roller plate assembly
	16	DXB1121	Bearing
	17	WT26D047D050	Washer
	18	DBK1023	G plate (L)
	19	DBK1024	G plate (R)

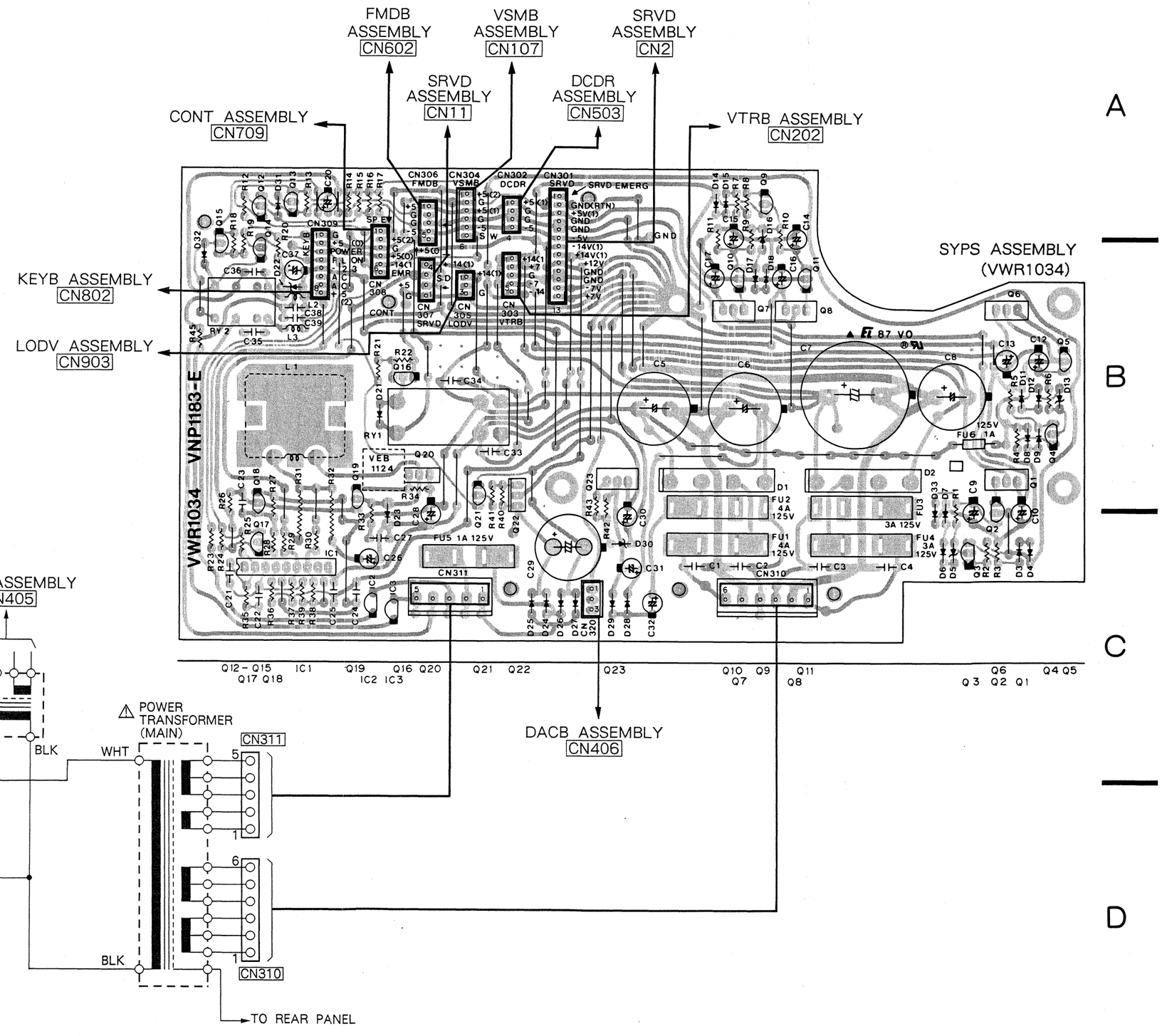
Mark	No.	Part No.	Description
	101		Lock teeth assembly
	102		Tilt base
	103		Slider
	104		PU holder
	105		Cord holder



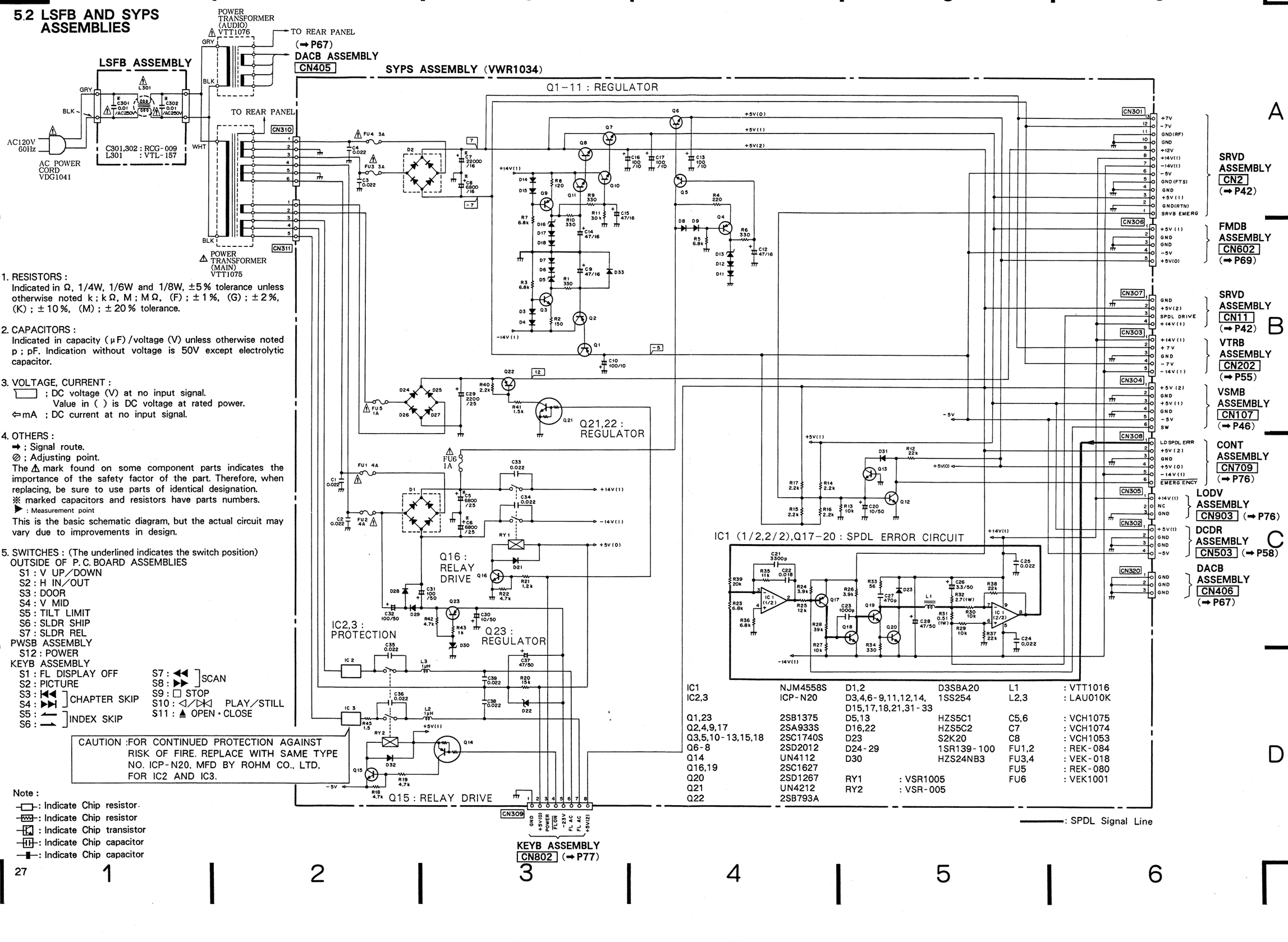
This P. C. B. connection diagram is viewed from the foil side.

P.C.B. pattern diagram indication	Corresponding part symbol	Part name	P.C.B. pattern diagram indication	Corresponding part symbol	Part name
		Transistor			Ceramic capacitor
		FET			Mylar capacitor
		Diode	SA		Styrol capacitor
			NP		Electrolytic capacitor (Non polarized)
		Zenner diode	NL		Electrolytic capacitor (Noiseless)
					Electrolytic capacitor (Polarized)
					Electrolytic capacitor (Polarized)
		LED			Power capacitor
		Varactor			Semi-fixed resistor
		Tact switch			Resistor array
					Resistor
		Inductor			
		Coil			Resonator
		Transformer			Thermistor
		Filter			

1. This P.C.B. connection diagram is viewed from the parts mounted side.
2. The parts which have been mounted on the board can be replaced with those shown with the corresponding wiring symbols listed in the above Table.
3. The capacitor terminal marked with ▭ shows negative terminal.
4. The diode marked with O shows cathode side.
5. The transistor terminal marked with ▭ shows emitter.



5.2 LSFB AND SYPS ASSEMBLIES



1. RESISTORS :
Indicated in Ω, 1/4W, 1/6W and 1/8W, ±5% tolerance unless otherwise noted k ; kΩ, M ; MΩ, (F) ; ±1%, (G) ; ±2%, (K) ; ±10%, (M) ; ±20% tolerance.

2. CAPACITORS :
Indicated in capacity (μF) / voltage (V) unless otherwise noted p ; pF. Indication without voltage is 50V except electrolytic capacitor.

3. VOLTAGE, CURRENT :
▭ ; DC voltage (V) at no input signal.
Value in ( ) is DC voltage at rated power.
⇦mA ; DC current at no input signal.

4. OTHERS :
➡ ; Signal route.
⊘ ; Adjusting point.
The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
※ marked capacitors and resistors have parts numbers.
▶ : Measurement point
This is the basic schematic diagram, but the actual circuit may vary due to improvements in design.

5. SWITCHES : (The underlined indicates the switch position)
OUTSIDE OF P.C. BOARD ASSEMBLIES
S1 : V UP/DOWN
S2 : H IN/OUT
S3 : DOOR
S4 : V MID
S5 : TILT LIMIT
S6 : SLDR SHIP
S7 : SLDR REL
PWSB ASSEMBLY
S12 : POWER
KEYB ASSEMBLY
S1 : FL DISPLAY OFF
S2 : PICTURE
S3 : ⏮] CHAPTER SKIP
S4 : ⏭]
S5 : ⏪] INDEX SKIP
S6 : ⏩]
S7 : ◀◀] SCAN
S8 : ▶▶]
S9 : □ STOP
S10 : ◁/▷⏸ PLAY/STILL
S11 : ⏏ OPEN・CLOSE

CAUTION :FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE WITH SAME TYPE NO. ICP-N20, MFD BY ROHM CO., LTD. FOR IC2 AND IC3.

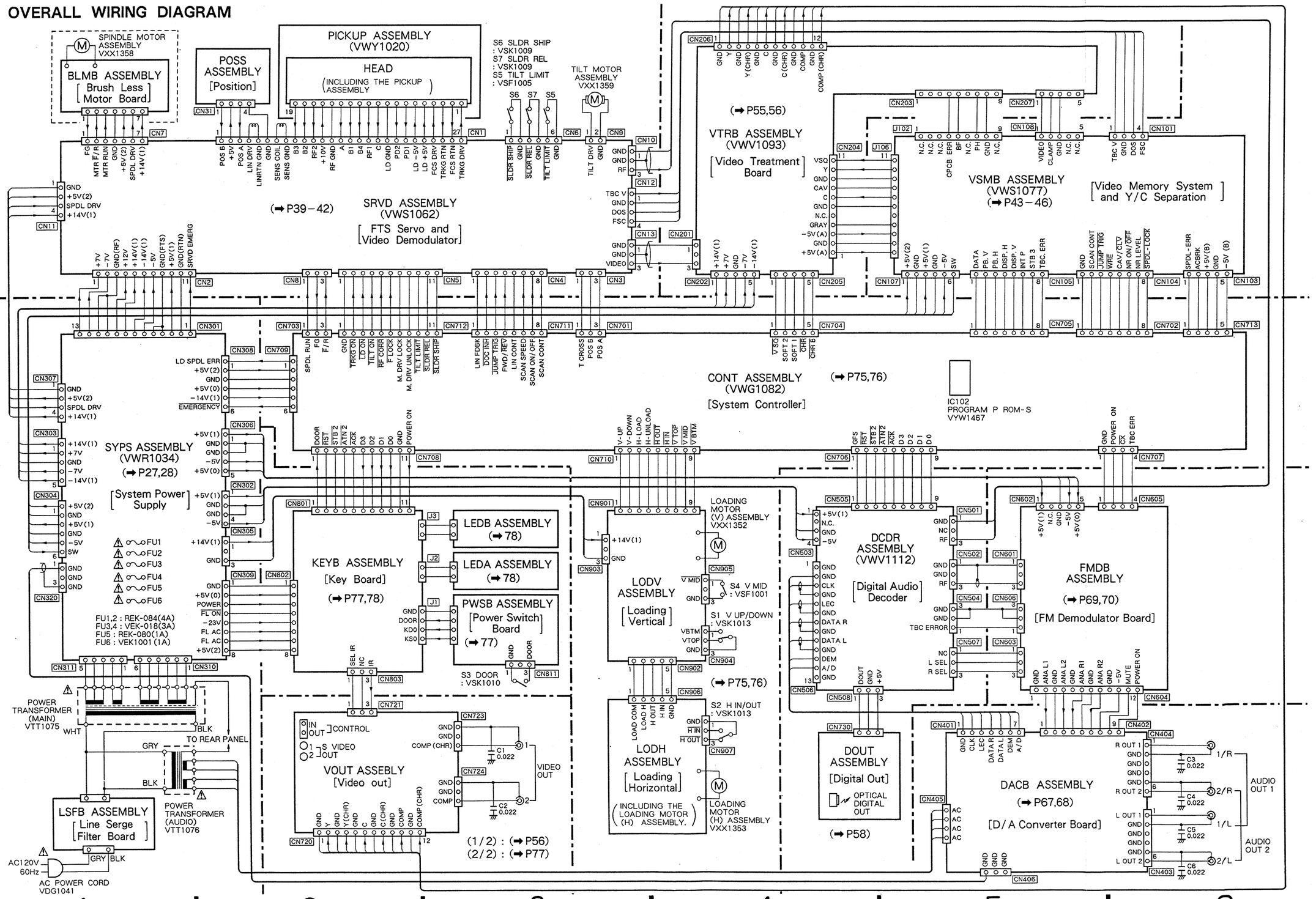
Note :
-□-: Indicate Chip resistor.
-▭-: Indicate Chip resistor
-⊣⊢-: Indicate Chip transistor
-||-: Indicate Chip capacitor
-|-: Indicate Chip capacitor

IC1	NJM4558S	D1,2	D3SBA20	L1	: VTT1016
IC2,3	ICP-N20	D3,4,6-9,11,12,14, D15,17,18,21,31-33	1SS254	L2,3	: LAU010K
Q1,23	2SB1375	D5,13	HZS5C1	C5,6	: VCH1075
Q2,4,9,17	2SA933S	D16,22	HZS5C2	C7	: VCH1074
Q3,5,10-13,15,18	2SC1740S	D23	S2K20	C8	: VCH1053
Q6-8	2SD2012	D24-29	1SR139-100	FU1,2	: REK-084
Q14	UN4112	D30	HZS24NB3	FU3,4	: VEK-018
Q16,19	2SC1627			FU5	: REK-080
Q20	2SD1267	RY1 : VSR1005		FU6	: VEK1001
Q21	UN4212	RY2 : VSR-005			
Q22	2SB793A				

——: SPDL Signal Line

5. SCHEMATIC AND P. C. BOARDS DIAGRAM

5.1 OVERALL WIRING DIAGRAM

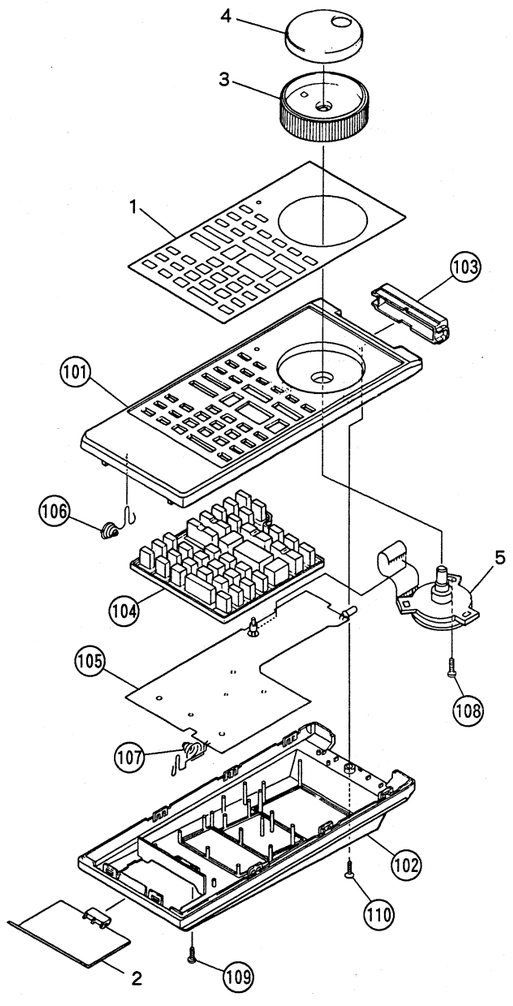


3.9 REMOTE CONTROL UNIT [CU-LD019 (VXX1370)]

Parts List of Remote Control Unit

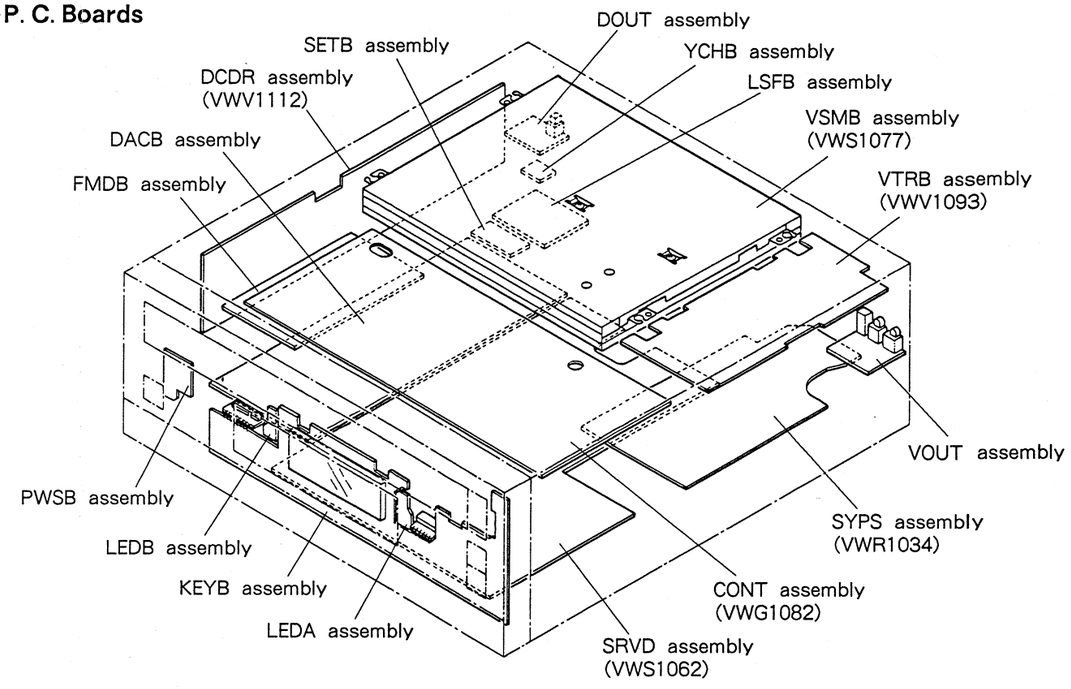
Mark	No.	Part No.	Description
	1	VAH1122	Alum. plate
	2	VNK1133	Battery cover
	3	VNK1395	Shuttle ring
	4	VNK1396	Jog dial
	5	VSD1006	Rotary encoder

Mark	No.	Part No.	Description
	101		Case (A)
	102		Case (B)
	103		Filter
	104		Contact rubber
	105		Remote control assembly
	106		Terminal (A)
	107		Terminal (B)
	108		Screw
	109		Screw
	110		Screw

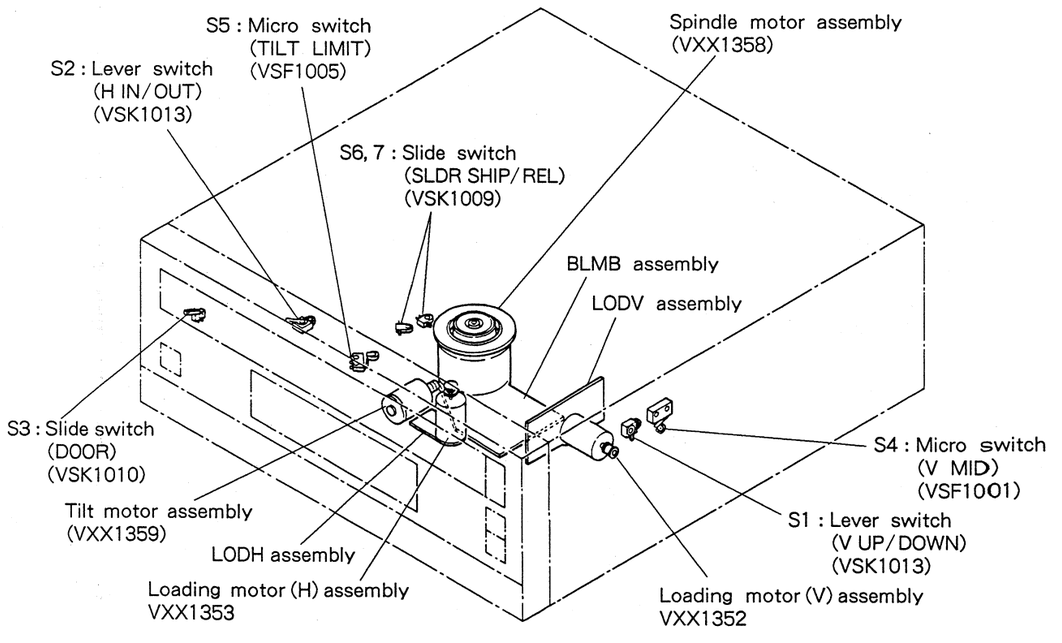


4. PARTS LOCATION

●P. C. Boards



●P. C. Boards, switches and motors



3.8 Pickup Assembly (VWY1020)

Parts List of Pickup Assembly

Mark	No.	Part No.	Description
	1	VED-034	Pad
	2	VNH1025	Actuator cover
	3	VGX-071	Magnetic circuit assembly
	4	VEB1012	Insulation sheet
	5	VGX-069	Objective lens assembly
	6		• • • • •
	7	VLL-292	Screw 5
	8	PBE-020	Wave washer (4)
	9	VGX-064	Multi lens assembly
	10		• • • • •
	11	VGX1010	PD-HEAD assembly
	12		• • • • •
	13		• • • • •
	14	PBE-022	Wave washer (8)
	15	VGX1004	LD assembly
	16	VEX1001	Sensor assembly
	17	VNH-056	Sensor stay
	18		• • • • •
	19	VDA1017	Fuji card
	20	VGX1005	Wave length plate assembly
	21	PBM20P120FMC	Screw
	22	PMA20P140FMC	Screw
	23	PMA20P080FMC	Screw
	24	WA40F100M050	Washer
	25	PPZ20P050FMC	Screw
	26	PMB20P050FMC	Screw
	27	PBZ20P080FMC	Screw
	28	PMA26P080FMC	Screw
	29	WA20W050R050	Washer
	30	PMA20P040FMC	Screw
	31	PMA26P060FMC	Screw
	101		• • • • •
	102		Optical body
	103		Prism assembly
	104		PD spring N

INSTALLING THE HEAD ASSEMBLY

The Head assembly is supplied with the flexible parts not bent ; therefore, use the following procedure to process.

1. Bend as shown by the arrow in Fig. 1 and fasten using double-sided tape and adhesive.
2. With the flexible parts bent as shown in Fig. 1, mount on the pick-up.
3. Mount the flex strip that connects the disc tilt detection PCB and the TRKG and FOCS coils on the Head assembly as shown in Fig. 2.

Note :

The copper foil of the flex strip has little resistance to heat ; therefor, soldering should be performed as quickly as possible. Apply the soldering iron to the Head assembly, not to the flex strip.

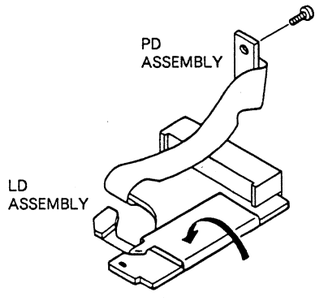


Fig. 1

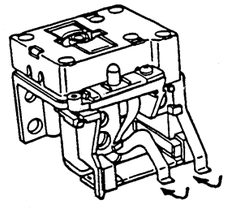
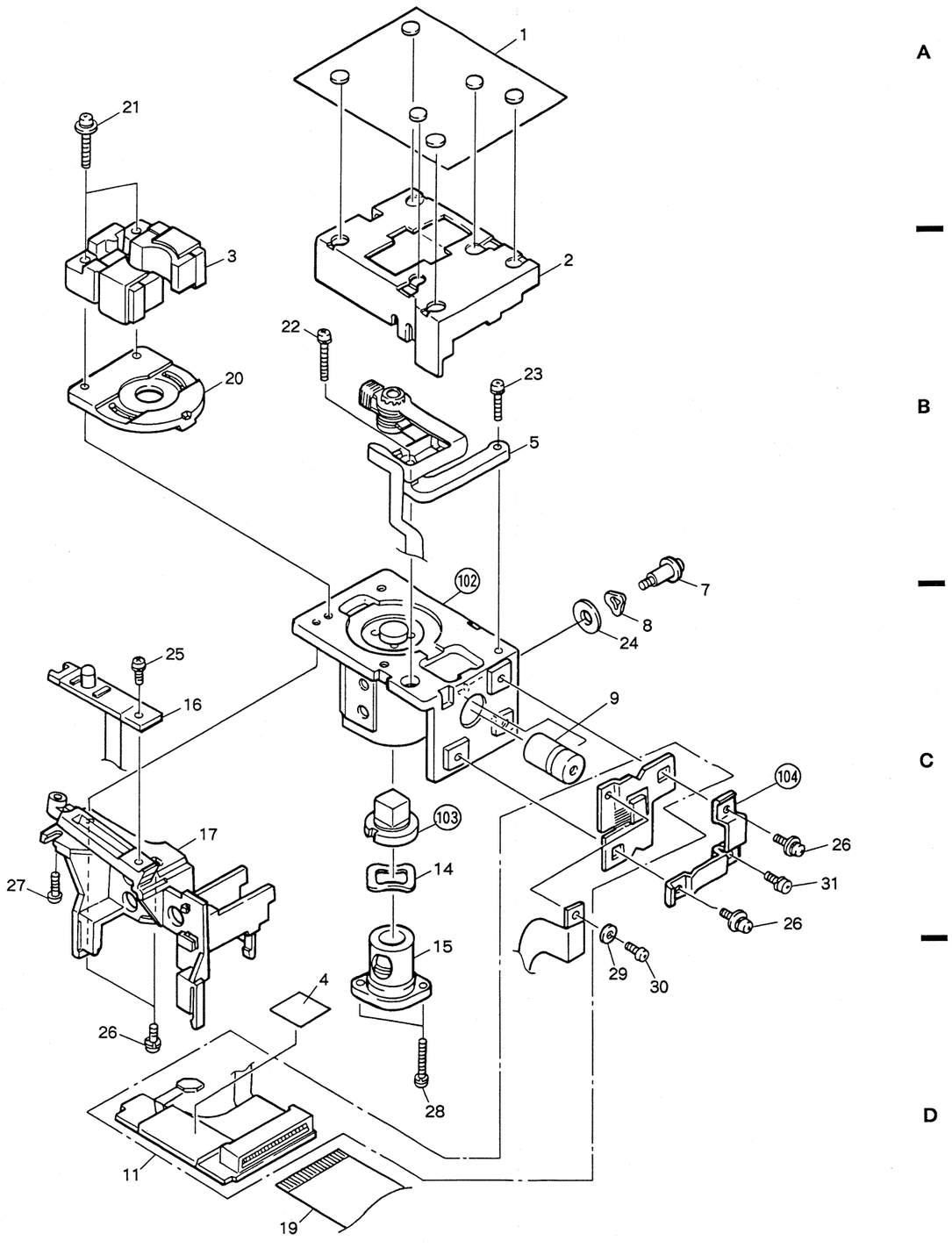
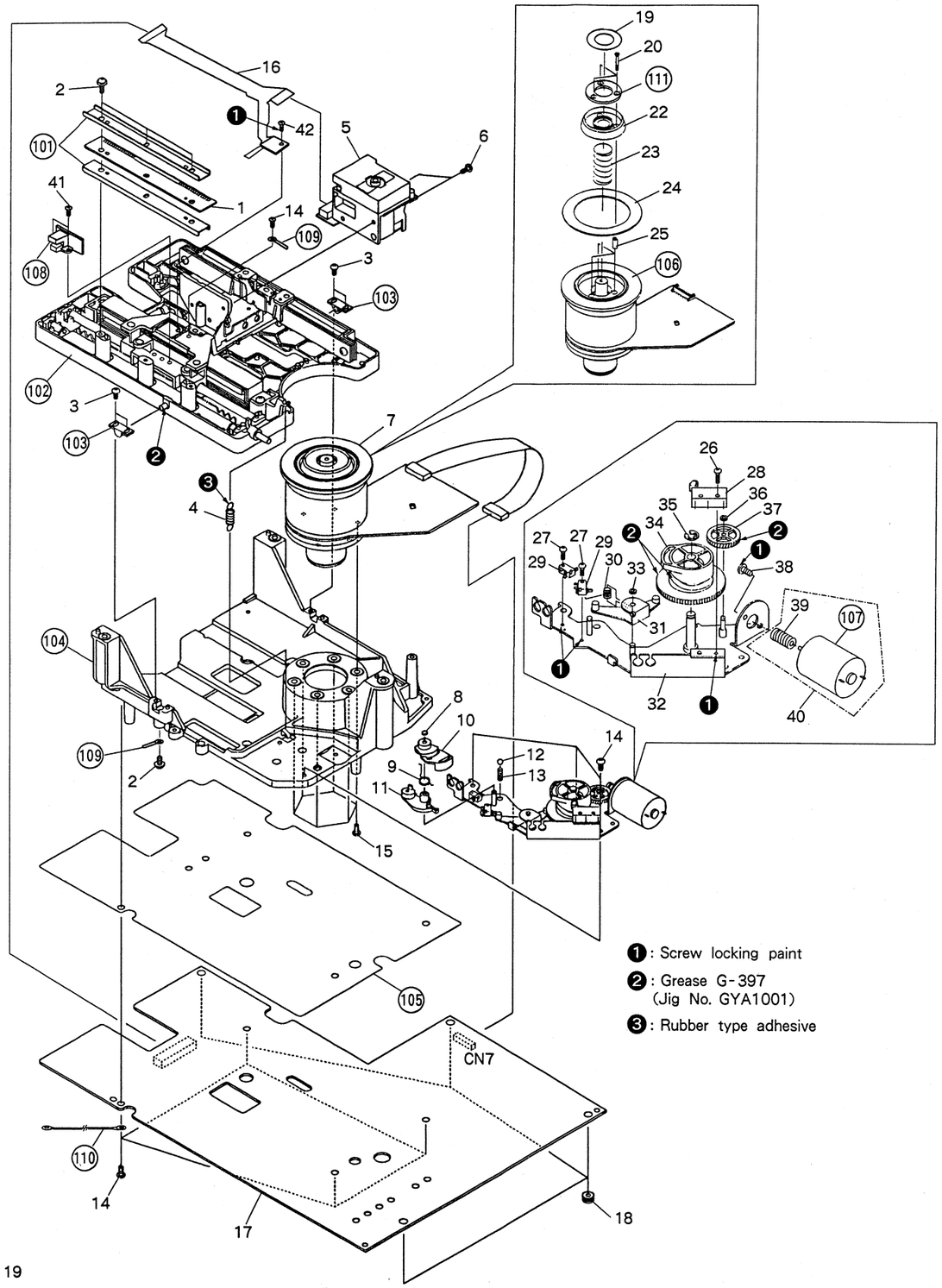


Fig. 2



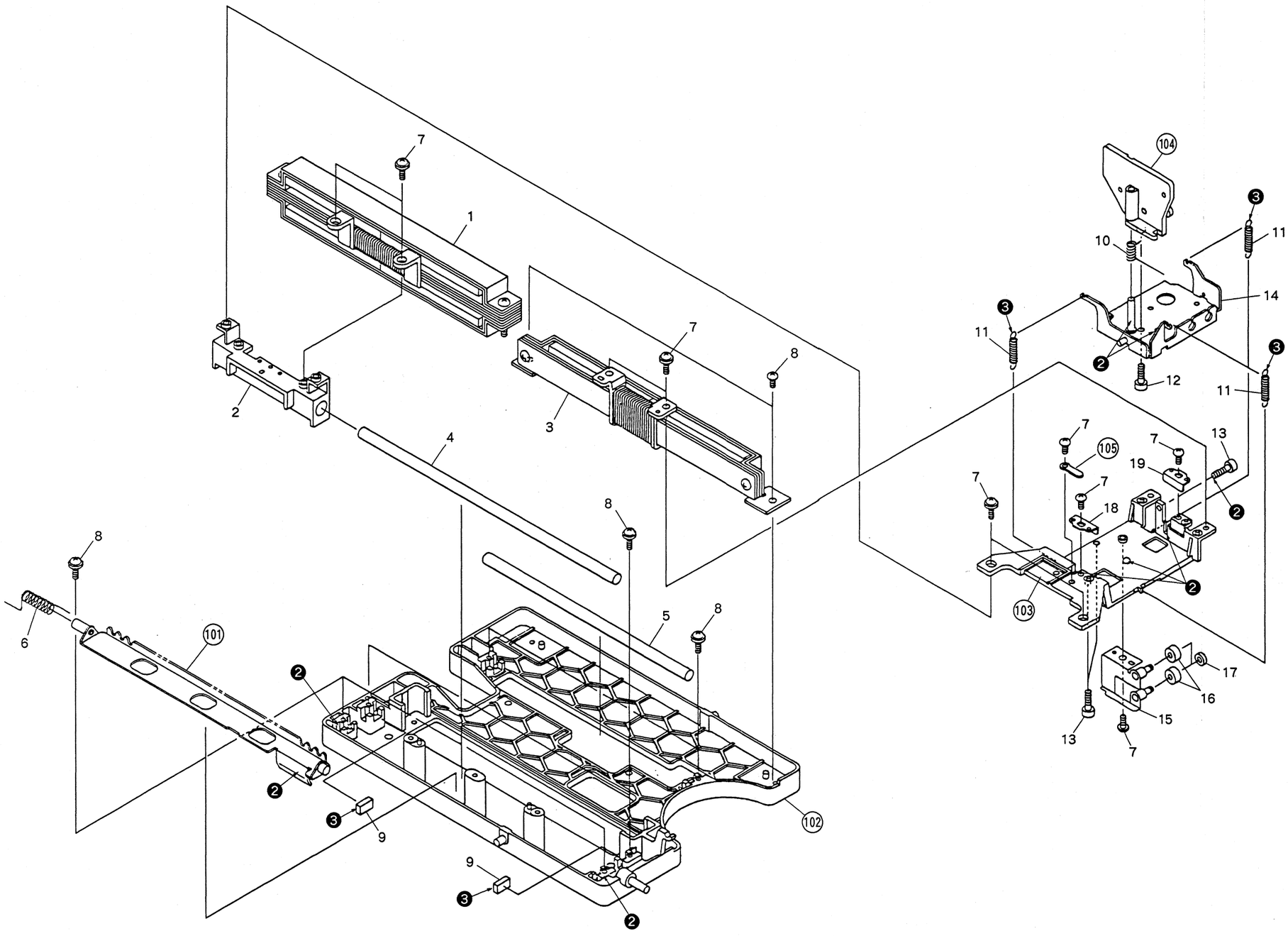
3.7 MECHANISM SECTION



Parts List of Mechanism Section

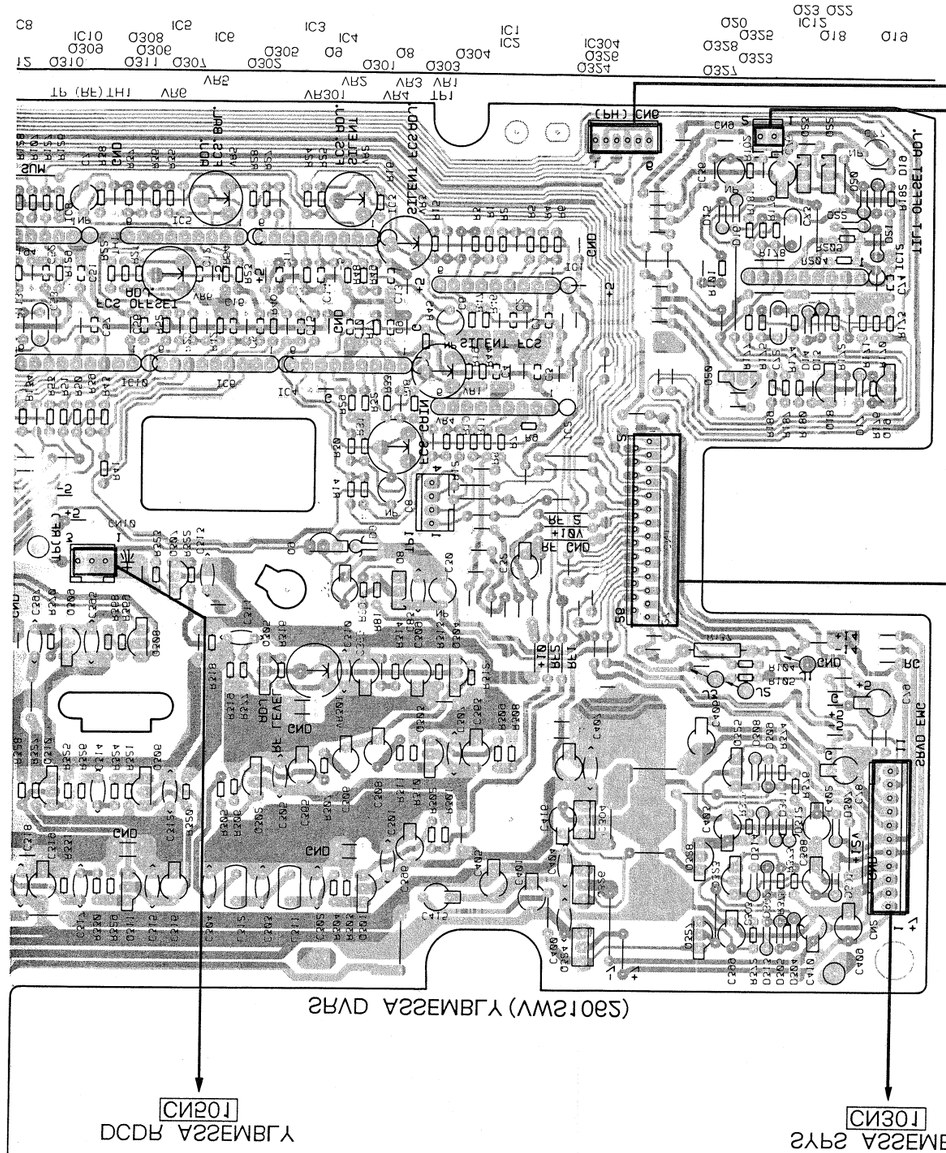
Mark	No.	Part No.	Description
	1	DNH1166	Slit plate
	2	IBZ30P080FCC	Screw
	3	PMH30P120FCU	Screw
	4	VBH1110	Tilt spring
	5	VWY1020	Pickup assembly
	6	PMB26P060FCU	Screw
	7	VXX1358	Spindle motor assembly
	8	WT21D050D050	Washer
	9	VBH1124	Cam spring
	10	VNL1276	Lock cam (B)
	11	VNL1274	Lock cam (A)
	12	VNH-026	Steel ball (ϕ 4)
	13	VBH1112	Ball spring
	14	PMB30P060FCU	Screw
	15	PMB30P080FCU	Screw
	16	VNP1194	Flexible card
◉	17	VWS1062	SRVD assembly
	18	VEB1113	Rubber bushing (C)
	19	VEC1279	Gap sheet
	20	CMZ20P140FMC	Screw
	21		• • • • •
	22	VLL1261	Centering hab
	23	VBH1114	Centering spring
	24	VEB1008	Rubber spacer
	25	VLL1266	Collar (A)
	26	AMZ20P080FCU	Screw
	27	BMZ20P060FCU	Screw
	28	VSF1005	Micro switch (S5) (TILT LIMIT)
	29	VSK1009	Slide switch (S6, 7) (SLDR SHIP/REL)
	30	VBH1111	Lever spring
	31	VXA1396	Lever assembly
	32	VXA1395	Lock base assembly
	33	WT21D050D050	Washer
	34	VNL1273	Tilt cam
	35	YE40FUC	Washer
	36	WT21D050D050	Washer
	37	VNL1078	Gear
	38	BMZ30P030FCU	Screw
	39	VNL1085	Worm
	40	VXX1359	Tilt motor assembly
	41	AMZ20P040FCU	Screw
	42	VBB1001	Rosin screw

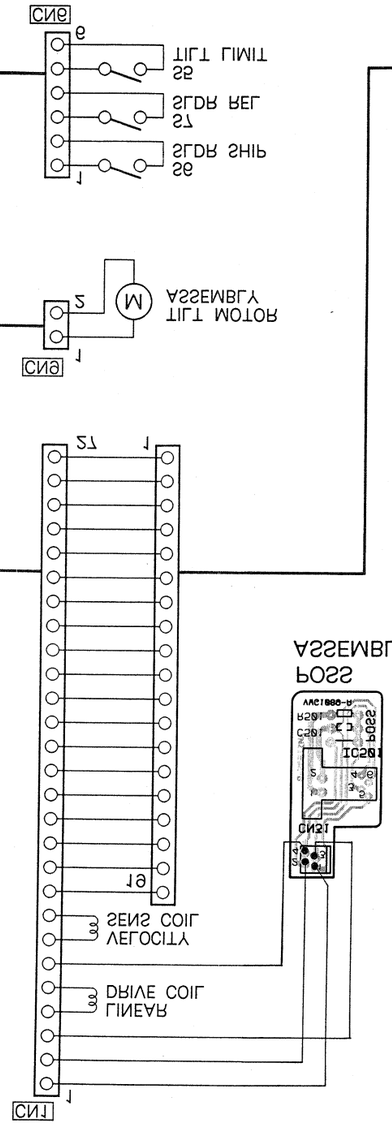
Mark	No.	Part No.	Description
	101		Reinforced plate
	102		Tilt base assembly
	103		Optical holder
	104		Mechanism chassis
	105		Insulation sheet
	106		Spindle motor
	107		Tilt motor
	108		POSS assembly
	109		Cord holder
	110		Earth lug assembly
	111		Yoke plate

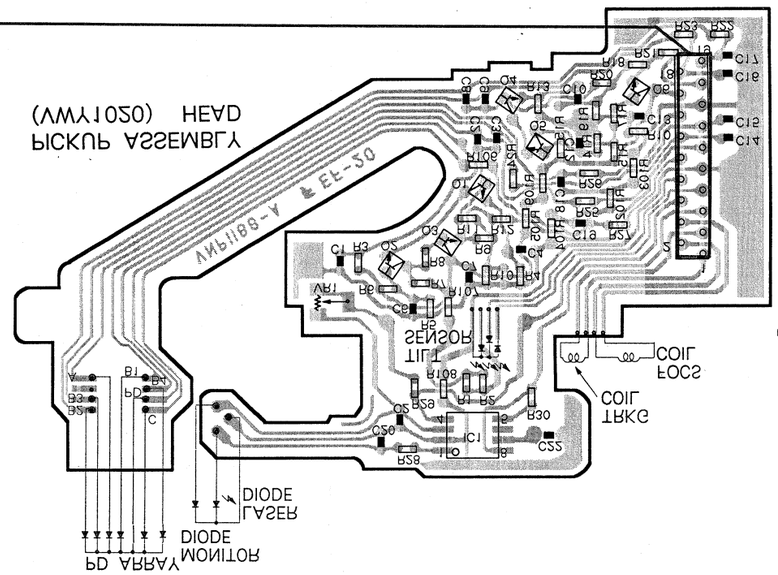


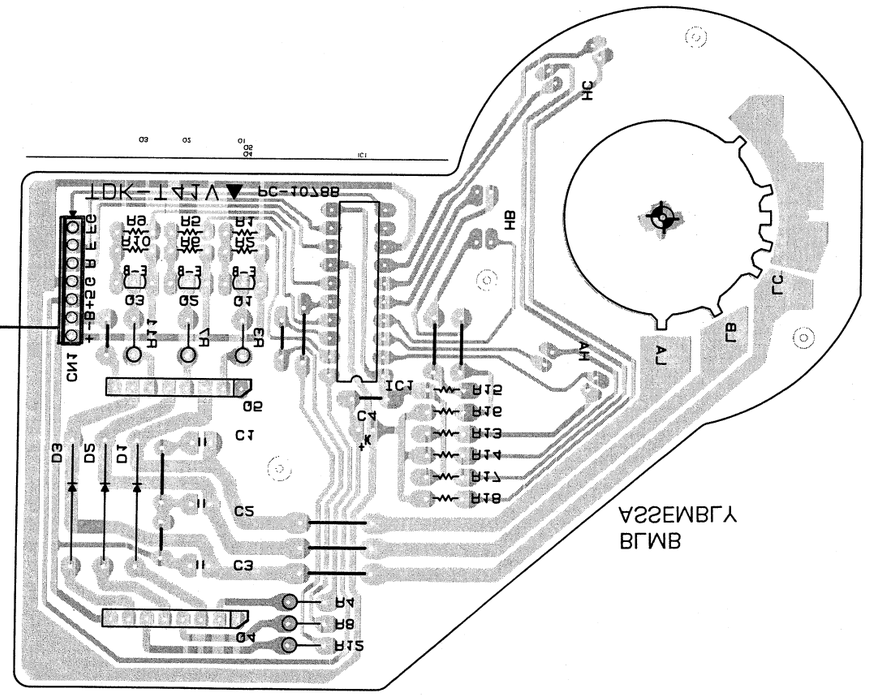
❷ : Grease G-397 (Jig No. GYA1001)

❸ : Rubber type adhesive

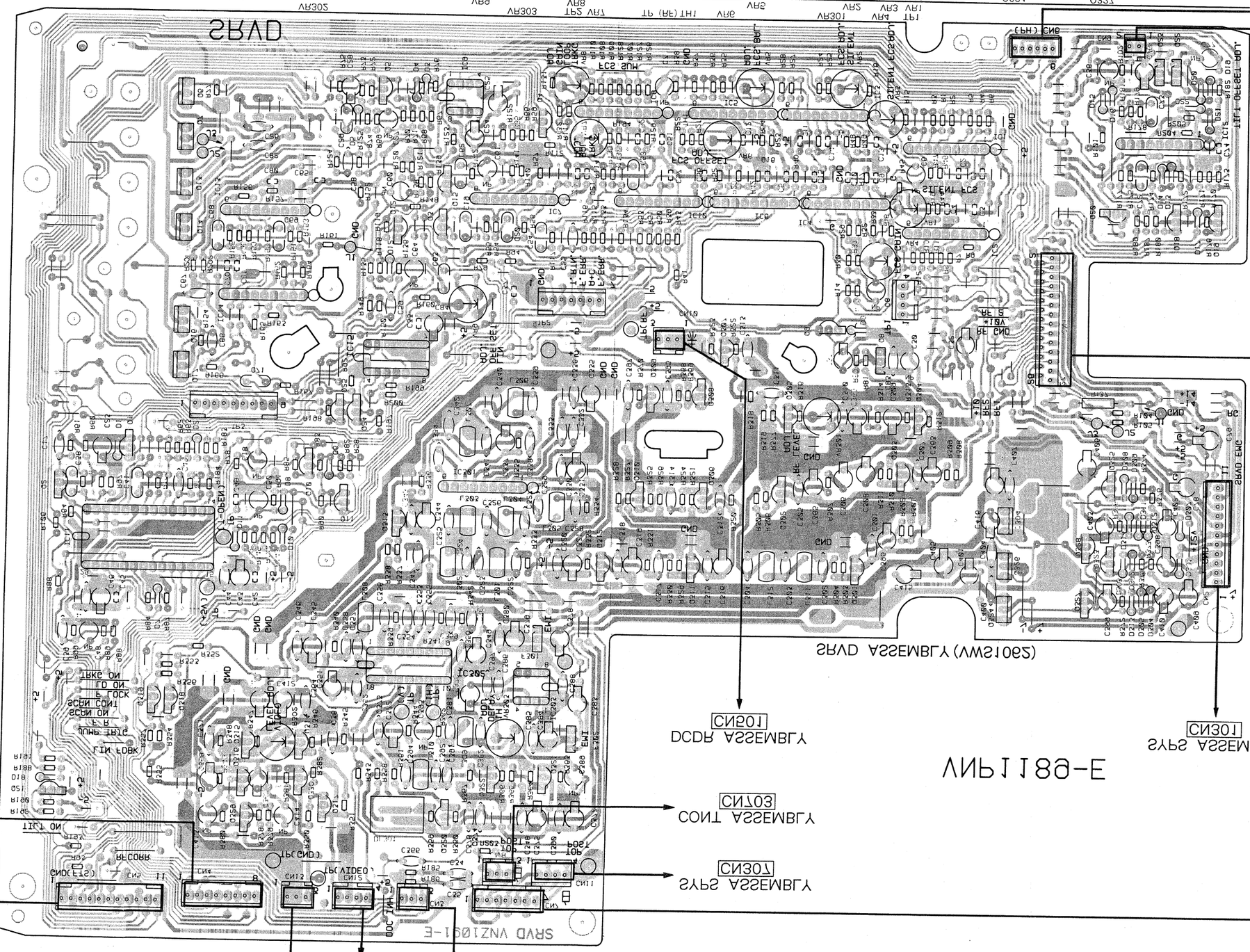








This P. C. B. connection diagram is viewed from the foil side.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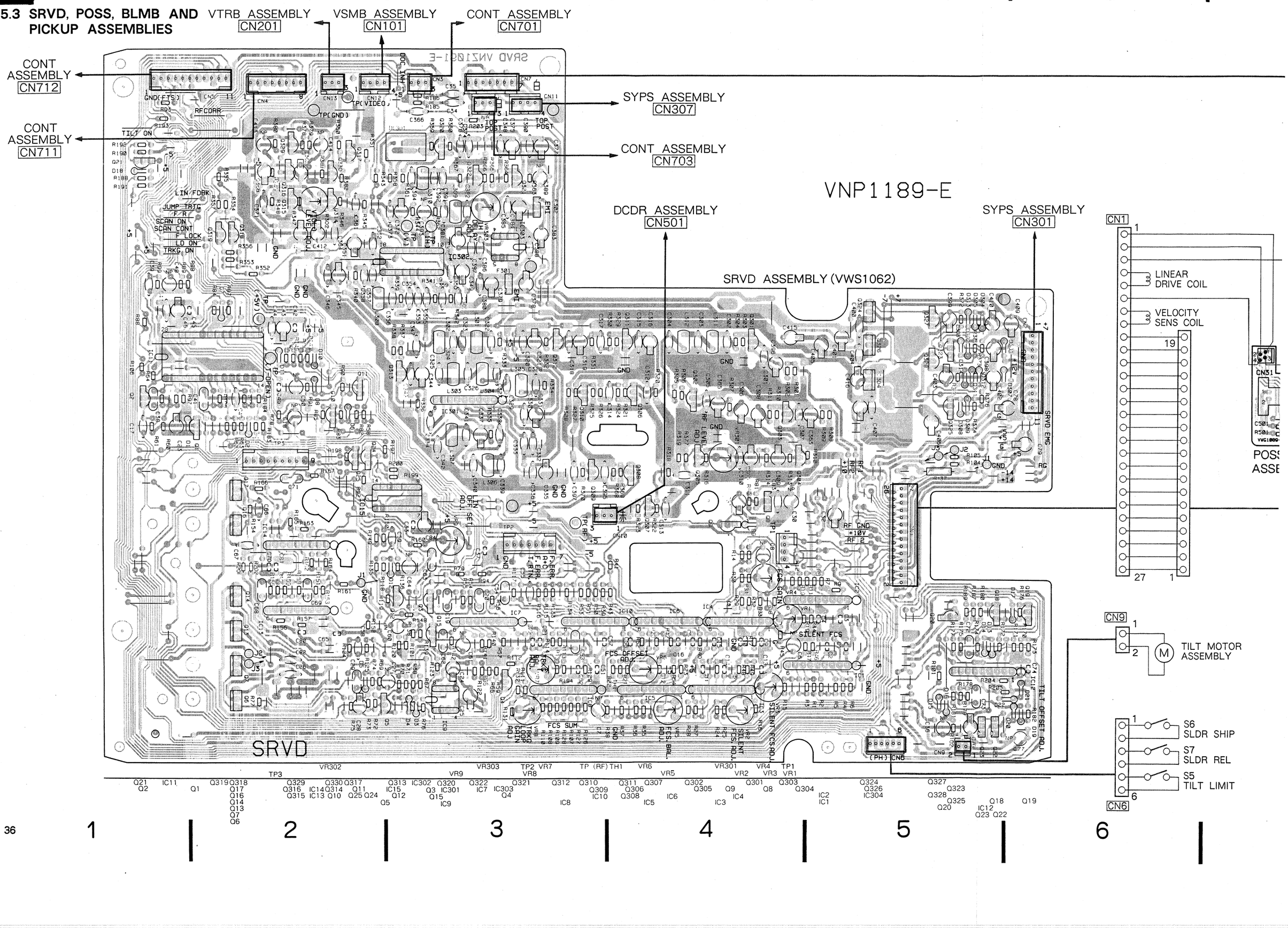
SRVD ASSEMBLY (SW1305)
DCDR ASSEMBLY

5.3 SRVD, POSS, BLMB AND PICKUP ASSEMBLIES



SYPS ASSEMBLY
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SYPS ASSEMBLY
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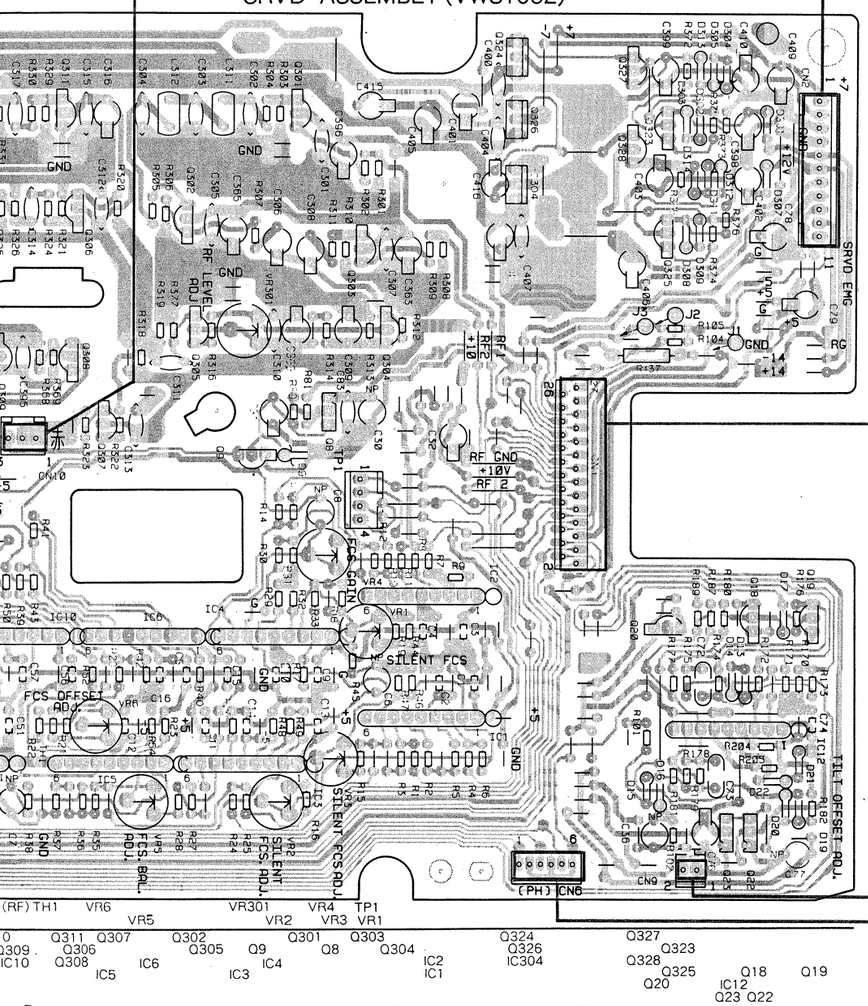
SRVD ASSEMBLY (VWS1062)



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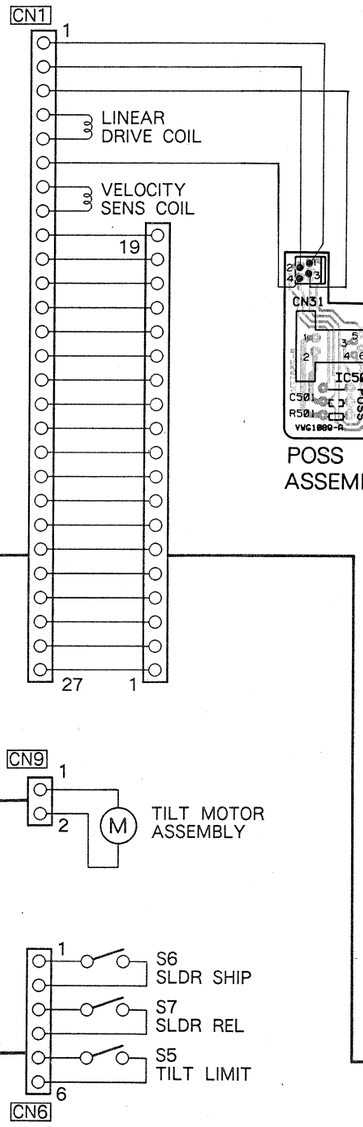

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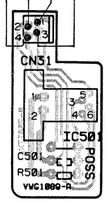
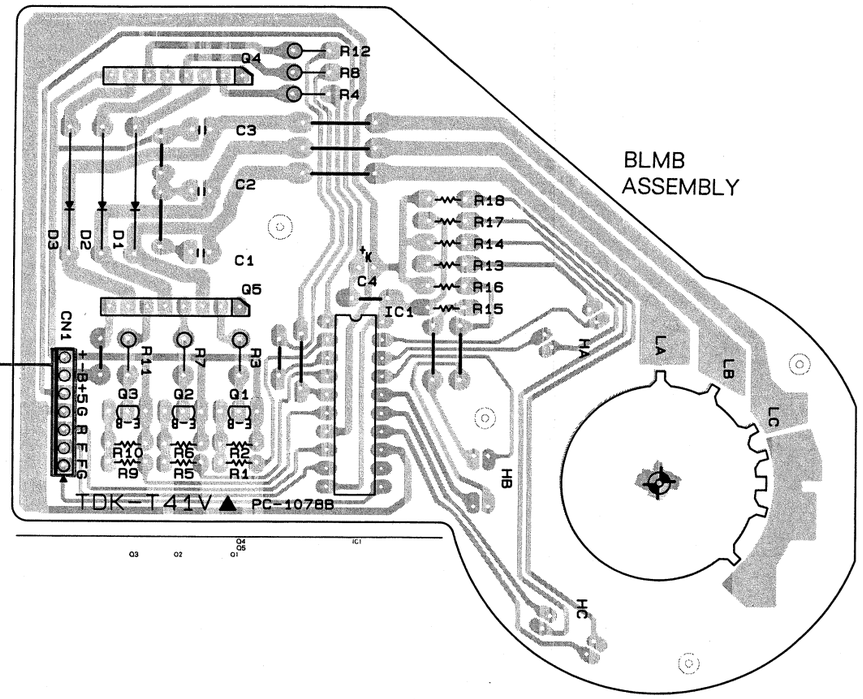
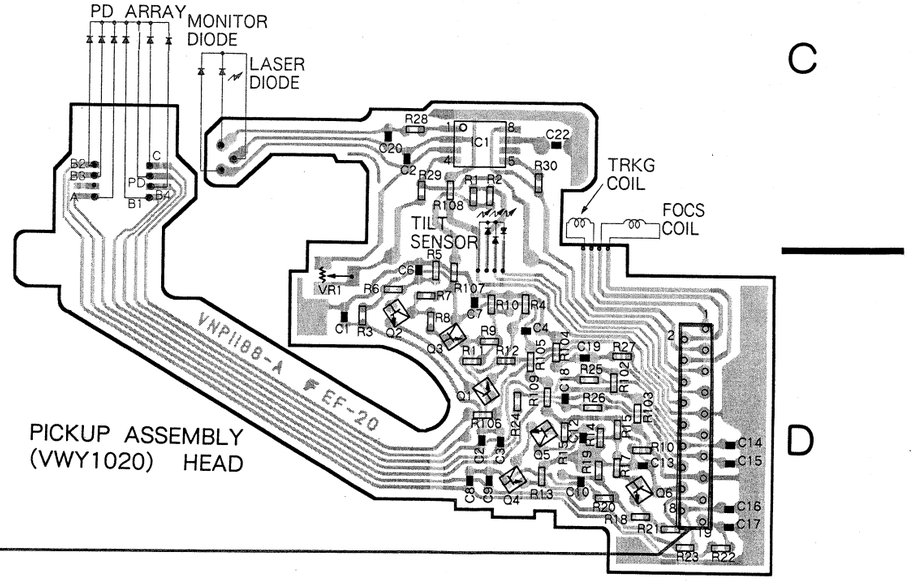


POSS ASSEMBLY

CN9

CN6





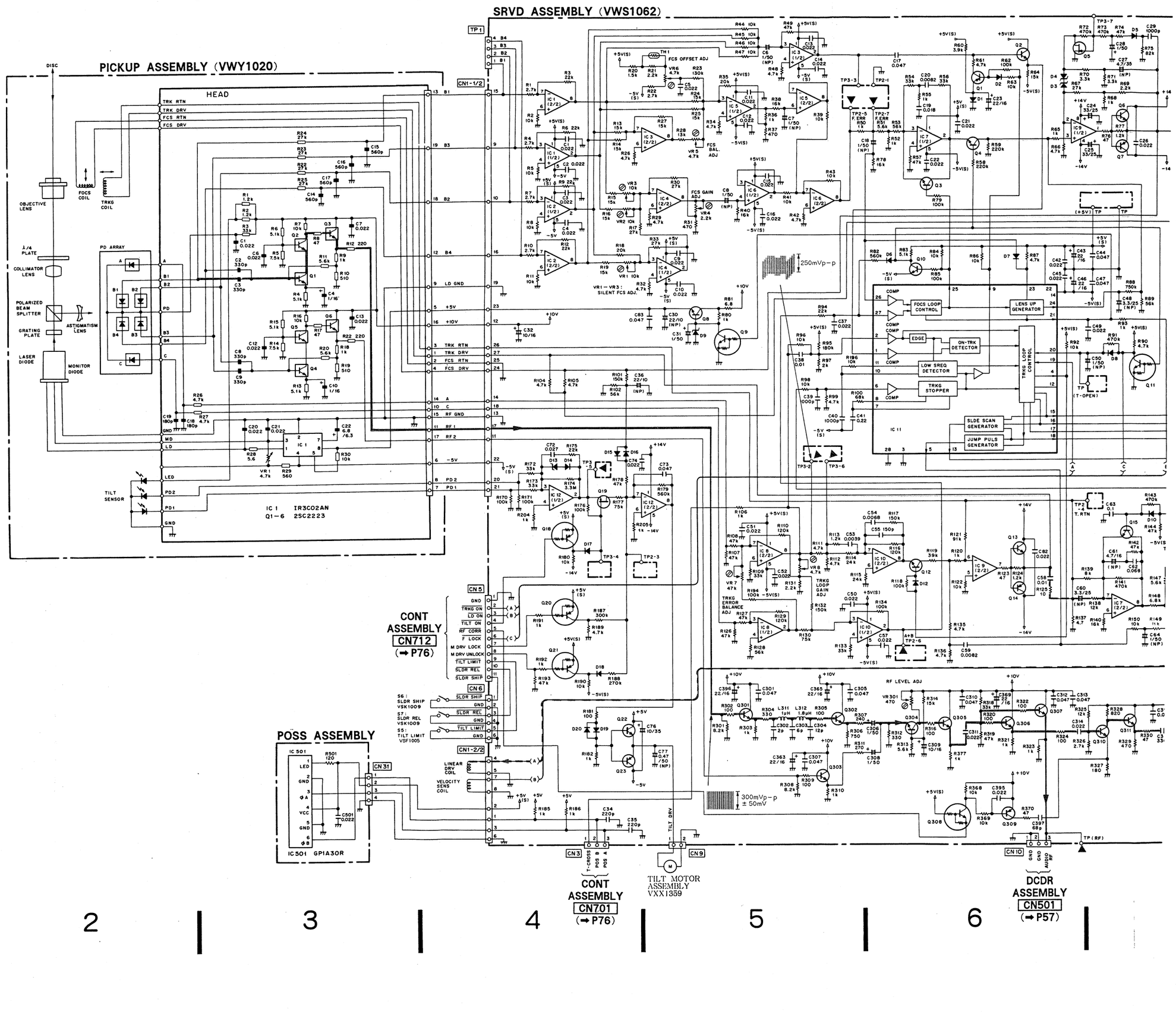
A

B

C

D

4 5 6 7 8 9


PICKUP ASSEMBLY (VWY1020)
HEAD
TRK RTN
TRK DRV
FCS RTN
FCS DRV
DISC
OBJECTIVE LENS
FOCS COIL
TRKG COIL
λ/4 PLATE
COLLIMATOR LENS
POLARIZED BEAM SPLITTER
GRATING PLATE
LASER DIODE
ASTIGMATISM LENS
MONITOR DIODE
PD ARRAY
TILT SENSOR
IC 1 IR3C02AN
Q1–6 2SC2223
SRVD ASSEMBLY (VWS1062)
TP 1
CN1-1/2
FCS OFFSET ADJ
FCS BAL. ADJ
FCS GAIN ADJ
VR1 – VR3 : SILENT FCS ADJ.
250mVp-p
FOCS LOOP CONTROL
LENS UP GENERATOR
EDGE
ON-TRK DETECTOR
LOW SREQ DETECTOR
TRKG STOPPER
TRK6 LOOP GAIN CONTROL
SLDE SCAN GENERATOR
JUMP PULS GENERATOR
IC 11
TRKG ERROR BALANCE ADJ
TRKG LOOP GAIN ADJ
RF LEVEL ADJ
300mVp-p ± 50mV
(+5V) TP
(T-OPEN)
TP (RF)
CONT ASSEMBLY CN712 (➡P76)
CN 5
CN 6
S6 : SLDR SHIP VSK1009
S7 : SLDR REL VSK1009
S5 : TILT LIMIT VSF1005
CN1-2/2
LINEAR DRV COIL
VELOCITY SENS COIL
POSS ASSEMBLY
IC 501
IC501 GP1A30R
CN 31
CONT ASSEMBLY CN701 (➡P76)
CN3
T-CROSS POS B POS A
CN9
TILT MOTOR ASSEMBLY VXX1359
DCDR ASSEMBLY CN501 (➡P57)
CN10
GND GND AUDIO RF

7 8 9 10 11 12

A B C D

TH1	D33A	Q1,309,319,323,328	2SA933S	Q23	2SB1065	L301	: VTL1021
IC1,2	NJM082S	Q2 – 4,10,12,15,	2SC1740S	Q304,310	2SC1674	L302,303	: VTL-024
IC3 – 8,10	NJM4558S	Q301–303,305–307,				L304,305	: VTL1022
IC9	NJM4556DE	Q311–318,320–322,		D1,2,5–8,10–12,	1SS254	L306	: VTL1023
IC11	PM4001	Q325,327,329,330		D14–20,301–303,305,		L307	: VTL1024
IC12 – 14	NJM072SH	Q5,19	2SK184	D307–309,311,313,314		L308	: VTL-027
IC15	TC4066BP	Q6,13,16,324	2SD1762	D3,4	HZS3B3	L309,310	: VTL-042
IC301	PA0023	Q7,14,17,326	2SB1185	D9,13	MTZ5.6C	L311	: VTL-011
IC302	PA3018	Q8	2SD973A	D21,22	1SR139-100	L312	: VTL-014
IC303	PM0001	Q9,11,308	UN4212	D304,312	HZS5C1		
IC304	AN7810F	Q18,20,21,24,25	UN4112			F301,302	: VTH1012
		Q22	2SD1506				

VR1 – 3,9 : VRTB6VS103
VR4 : VRTB6VS222
VR5,6,8 : VRTB6VS472
VR7 : VRTB6VS473
VR301 : VRTG6VS471
VR302 : VRTG6VS222
VR303 : VRTG6VS102
DL301 : VTF-063

IC304 : REGULATOR

Q323–328 : REGULATOR

IC11 : FOCS/TRKG CONTROL

IC302 : 1H DELAY

IC301 : VIDEO DEMODULATOR

CN2 — SYPS ASSEMBLY CN301 (➡P28)
+7V, –7V, GND (RF), +12V, +14V (1), –14V (1), –5V, GND (FTS), +5V (1), GND (RTN), SRVD EMERG

CN4 — CONT ASSEMBLY CN711 (➡P76)
LINEAR FDBK, DOC INH, JUMP TRIG, FWD/REV, LINEAR CONT, SCAN SPEED, SCAN ON/OFF, SCAN CONT

CN12 — VSMB ASSEMBLY CN101 (➡P43)
TBC VIDEO, GND, DOS, FSC

CN13 — VTRB ASSEMBLY CN201 (➡P55)
GND, GND, VIDEO

CN7 — CONT ASSEMBLY CN703 (➡P75)
+14V (1), SPDL DRV, +5V (2), GND, MTR RUN, MTR F/R, FG

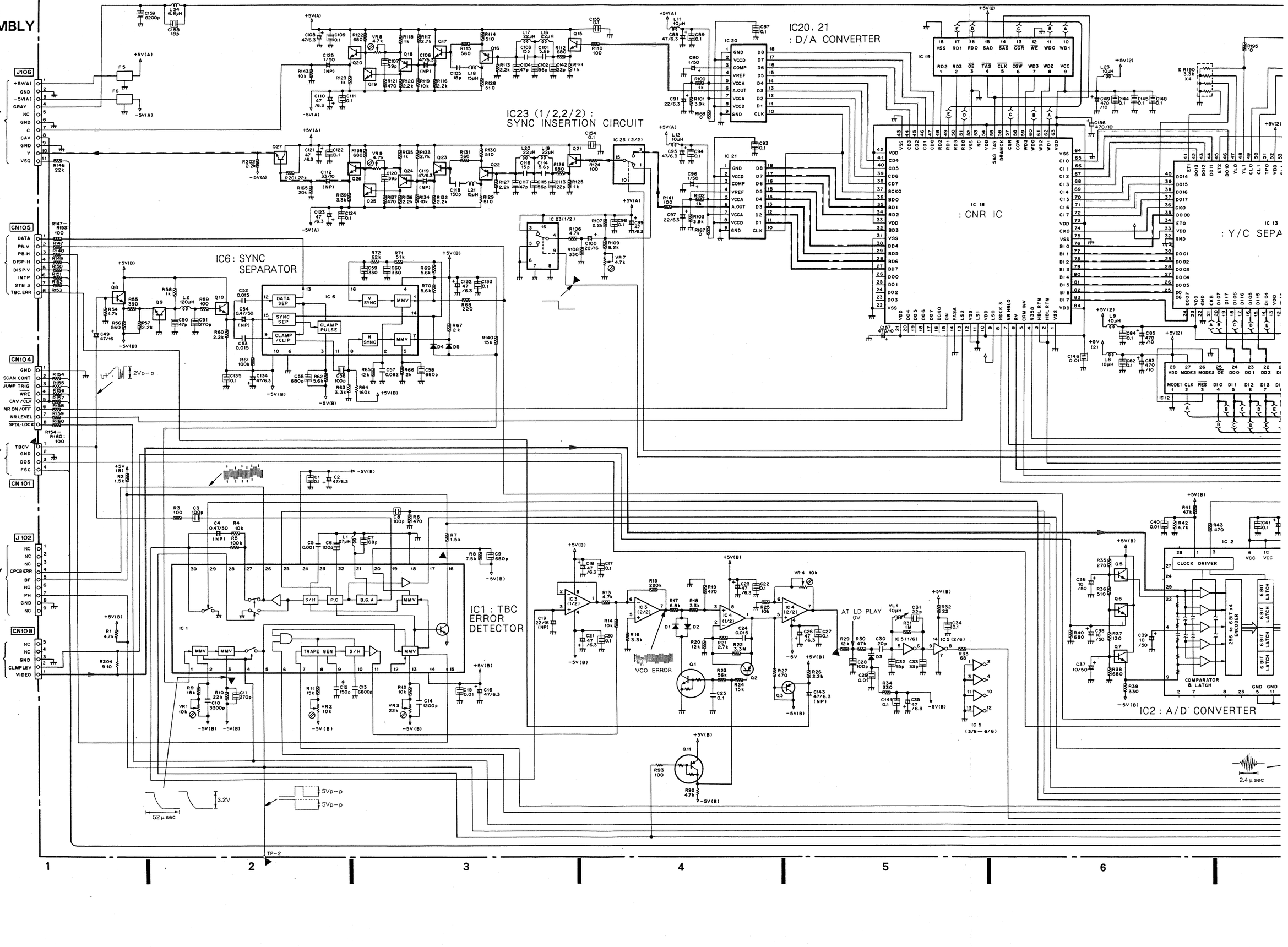
CN1 — SPINDLE MOTOR ASSEMBLY (VXX1358)
BLMB ASSEMBLY
Q5 STA303A
D1–3 S3V10
Z1 TA8413P
Q1–3 2SA817
Q4 STA302A
HA – HC : HALL DEVICE

CN8 — SPDL RUN, FG, MTR F/R
CN11 — GND, +5V (2), SPDL DRV, +14V (1)

: RF Signal Line
: Video Signal Line
: Linear Servo Line
: TRKG Servo Loop Line
: FOCS Servo Loop Line

5.4 VSMB ASSEMBLY

VSMB ASSEMBLY (VWS1077)



IC1	PA5012	Q1	UN4212
IC2	HA19211NT	Q2,3,14	2SA933S
IC3	NJM082D	Q4 – 10,15,17,	2SC2412K
IC4	NJM4558D	Q19 – 21,23,25 – 27	
IC5	TC74HCU04AP	Q11,12	DTA124ES
IC6	PA0009	Q13	2SC1740S
IC7	PDB005	Q16,18,22,24	2SA1037K
IC8	MN4760S		
IC9,10	MN4700	D1,2,4,5,7	1SS254
IC11	PDB006	D3	1SV68
IC12	HM63021P-34	D6	HZS2C2
IC13	PD5087		
IC14	TC9015P	VL1	: VTL1012
IC15	TC74HC74AP	L1	: LAU270J
IC16	TC74HC00AP	L2	: LAU121J
IC17	TC74HC164AP	L3	: LAU181J
IC18	PDB009	L4	: LAU120J
IC19	HM53051P-45	L5 – 9,11 – 12,22,23	: LAU100J
IC20 – 21	MB40778	L16,17,19,20	: LAU220J
IC23	TC74HC4053AP	L18,21	: LAU150J
		L24	: LAU6R8K
		L25	: LAU4R7K
		L101	: VTH1013

F1,5 – 8	: VTH1018
VC1	: VCM1002
C12	: VCE1022
VR1,2,4	: VRTB6VS103
VR3	: VRTB6VS223
VR5	: VRTB6VS102
VR7 – 9	: VRTG6VS472
R189,190	: RA4S332J

: Video Signal Line
: Video Data Signal Line
: SPDL Signal Line
: C Signal Line
: C Data Line
: Y Signal Line
: Y Data Line

IC13 : Y/C SEPARATION

IC14 : SYNC GENERATOR

IC2 : A/D CONVERTER

IC7 : TBC CONTROL

IC11 : MEMORY CONTROL

IC9,10 : 1MBIT VIDEO MEMORY

SYPS ASSEMBLY CN304 (➡ P28)

CONT ASSEMBLY CN713 (➡ P75)

CN107 CN103

DISP. V

DISP. H

VSQ

INTP

STB3

JUMP TRIG

SCAN CONT

CAV / CLV

WRE

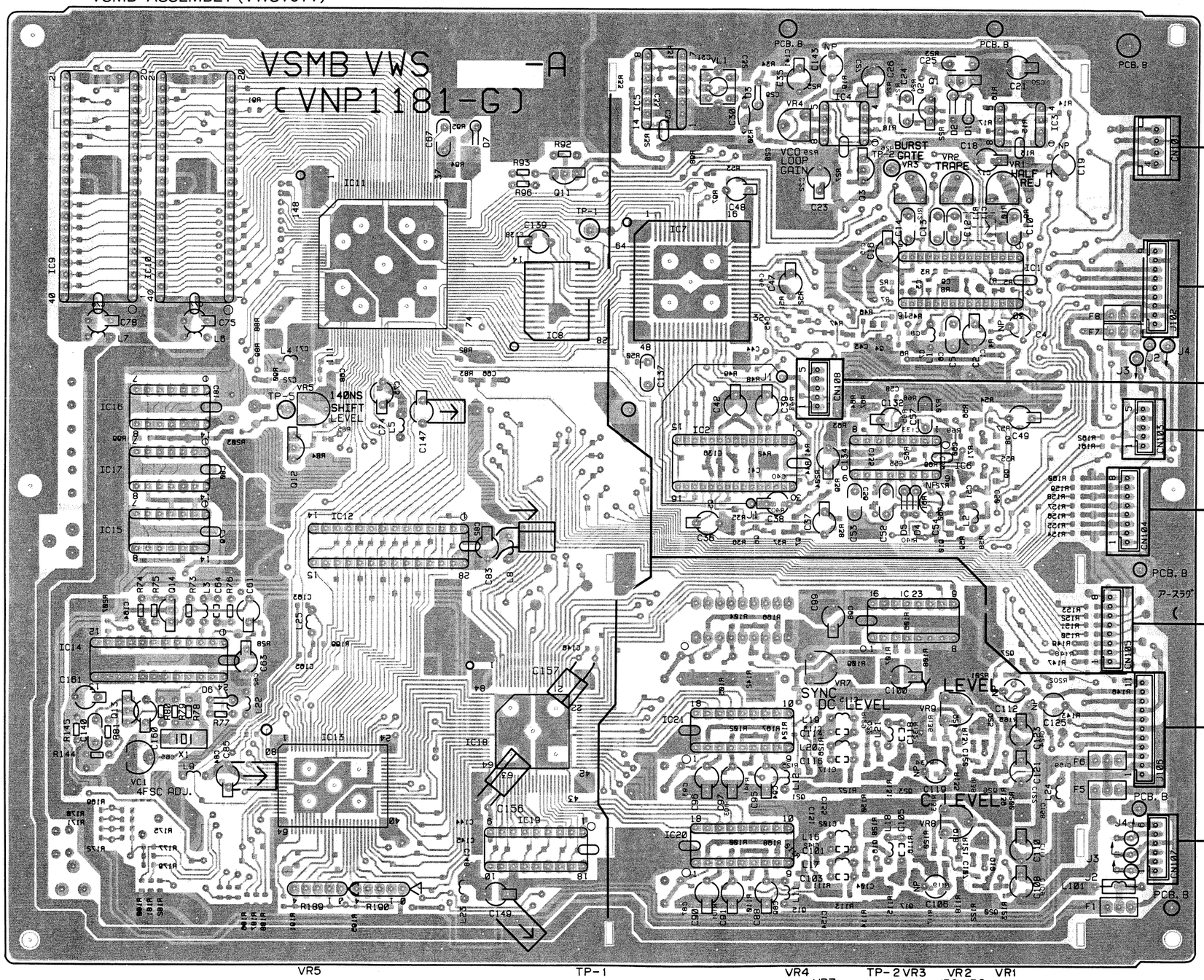
FSC

140msec±5msec

2.4μsec

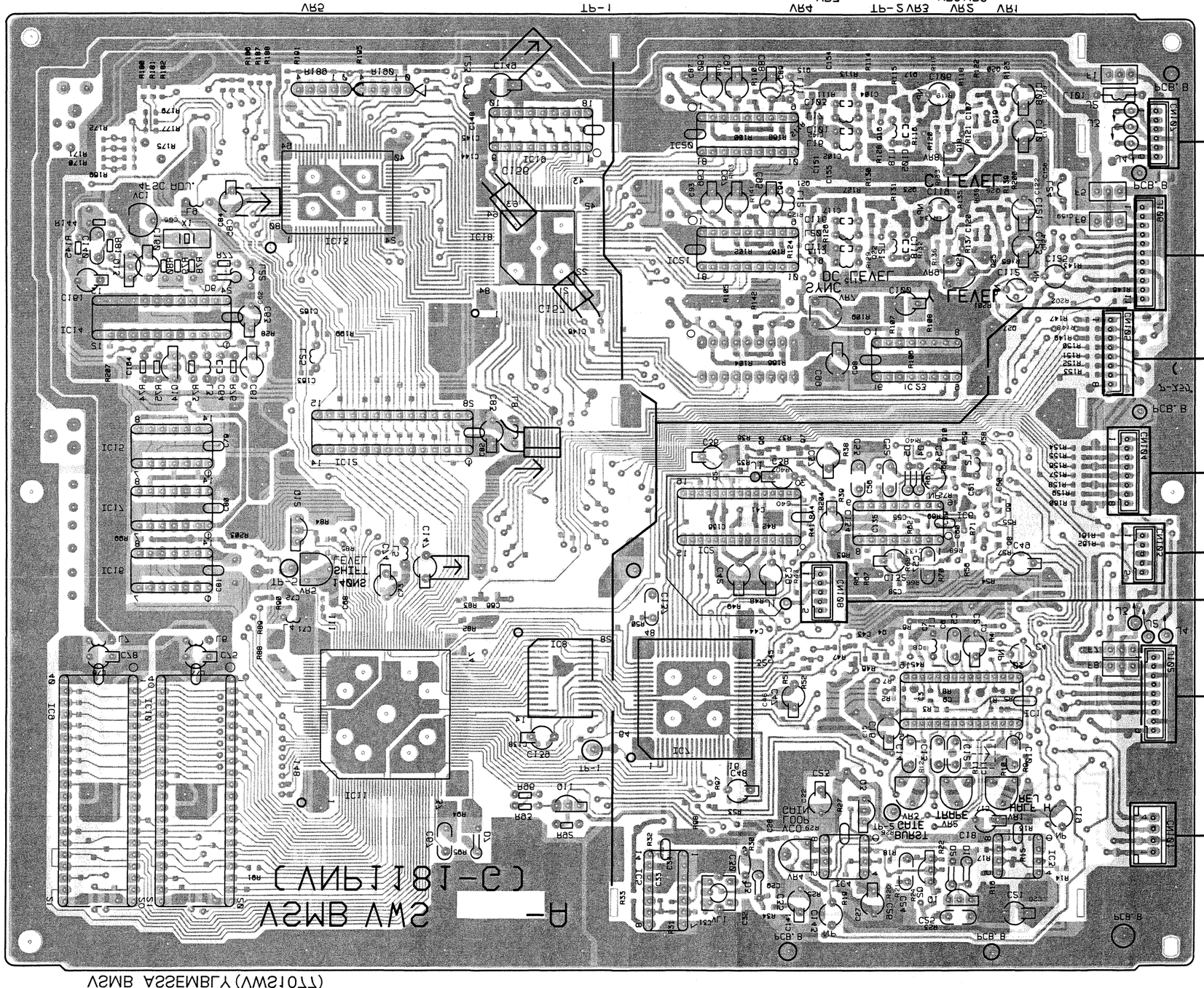
63μsec 4V

VSMB ASSEMBLY (VWS1077)



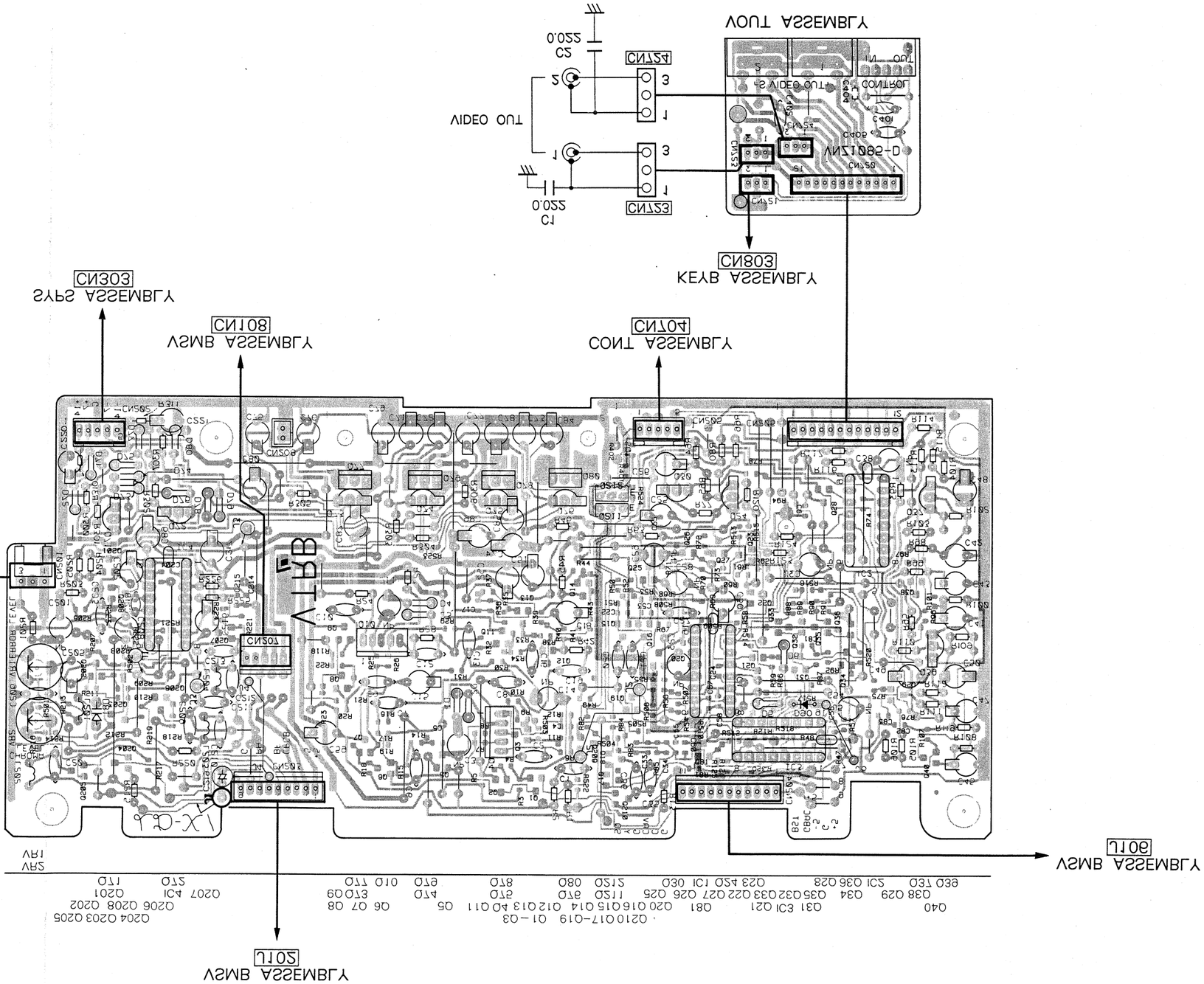
VR5 TP-1 VR4 VR7 TP-2 VR3 VR2 VR1 VR9 VR8

IC9 IC14 IC15 - IC17 IC10 Q13 Q14 Q12 IC11 IC12 IC13 Q11 IC8 IC18 IC19 IC5 IC7 IC2 IC21 IC20 IC4 IC6 IC23 Q1 IC1 IC3

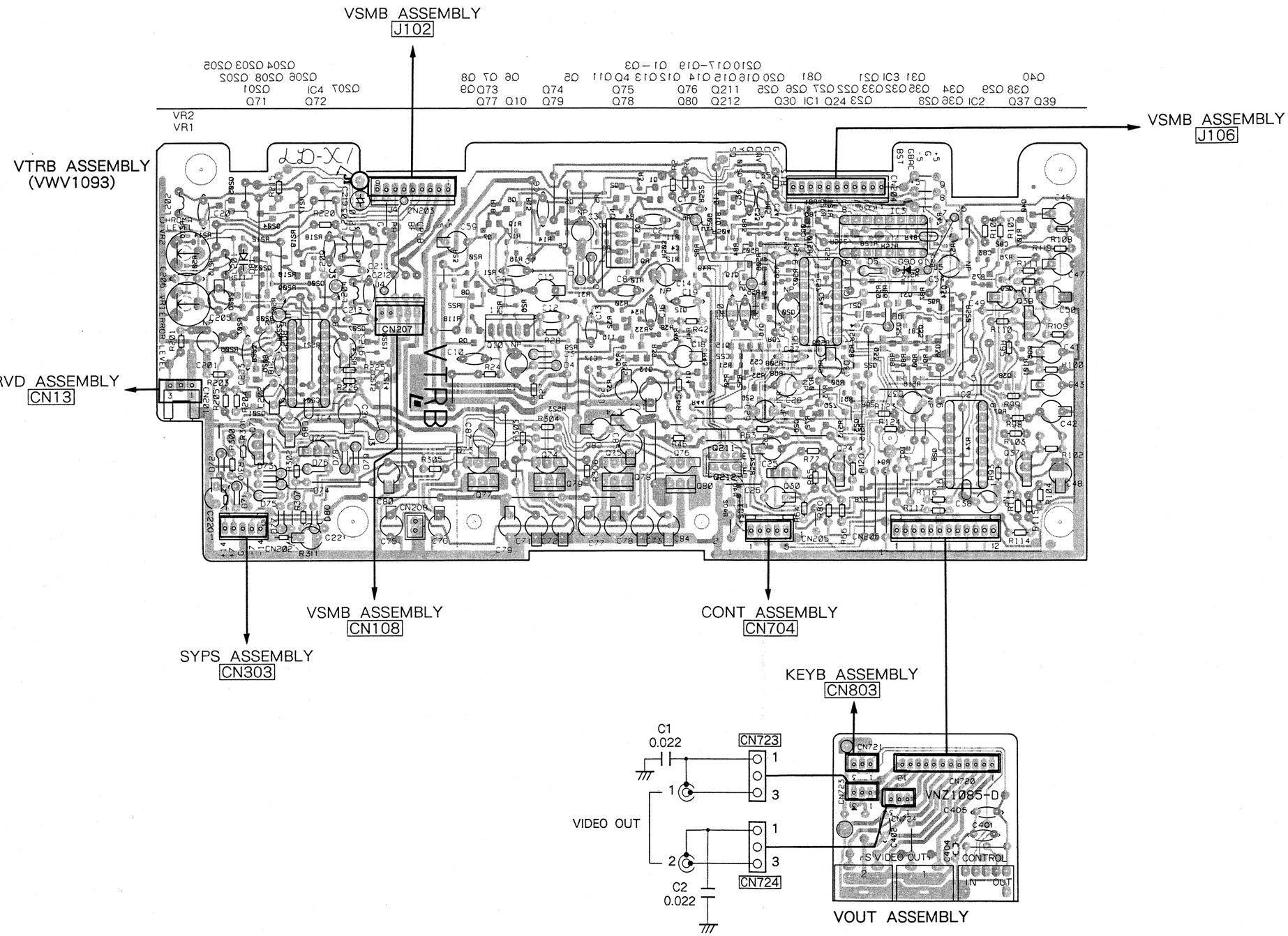

SYS'S ASSEMBLY
CN304
VTR ASSEMBLY
CN504
CONT ASSEMBLY
CN702
CONT ASSEMBLY
CN713
VTR ASSEMBLY
CN501
VTR ASSEMBLY
CN503
SYS ASSEMBLY
CN15
SYSW ASSEMBLY (SW-181 BOARD)
This P.C.B. connection diagram is viewed from the foil side.

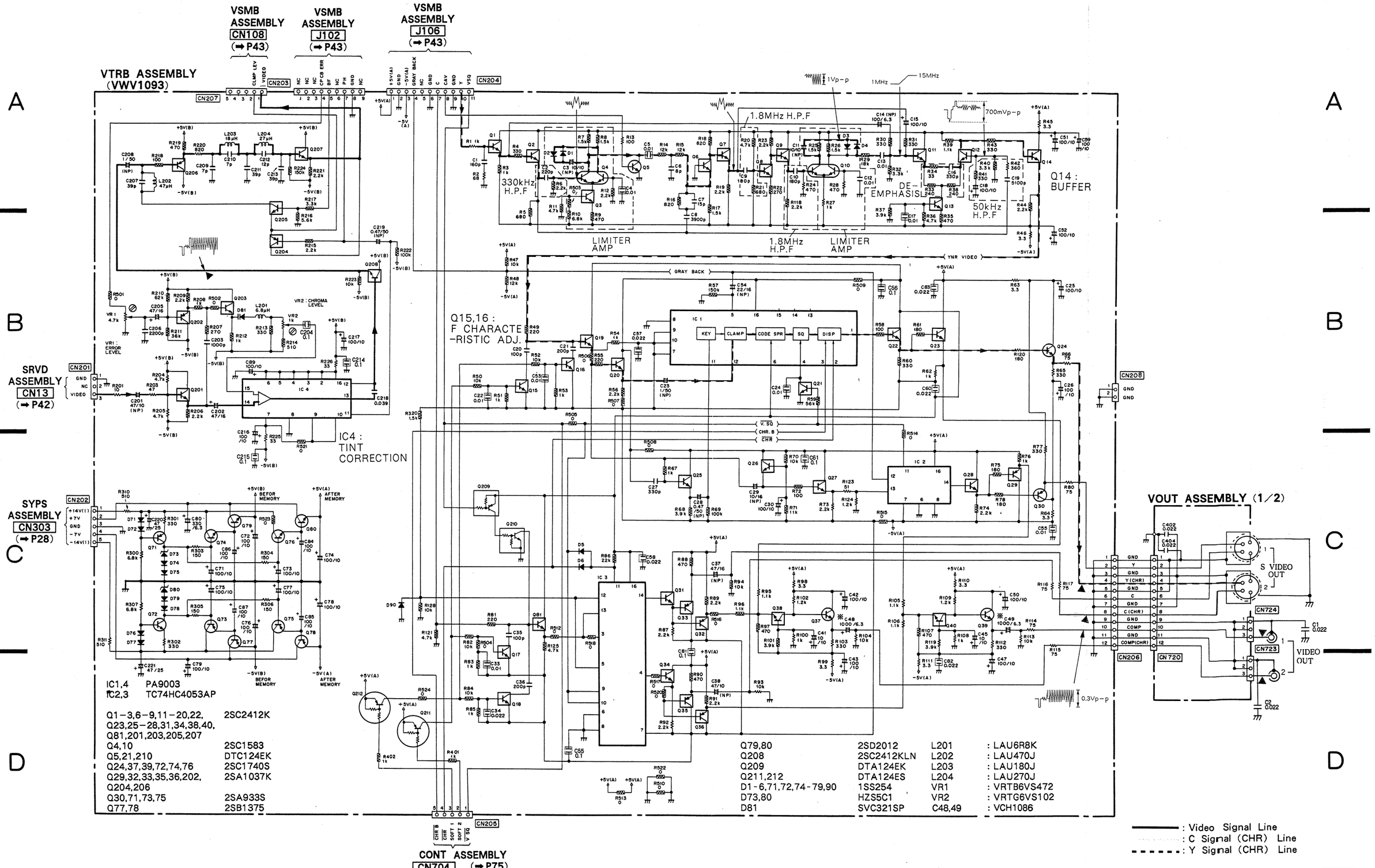
2.2 VTRB AND VOUT ASSEMBLIES

This P. C. B. connection diagram is viewed from the foil side.



5.5 VTRB AND VOUT ASSEMBLIES



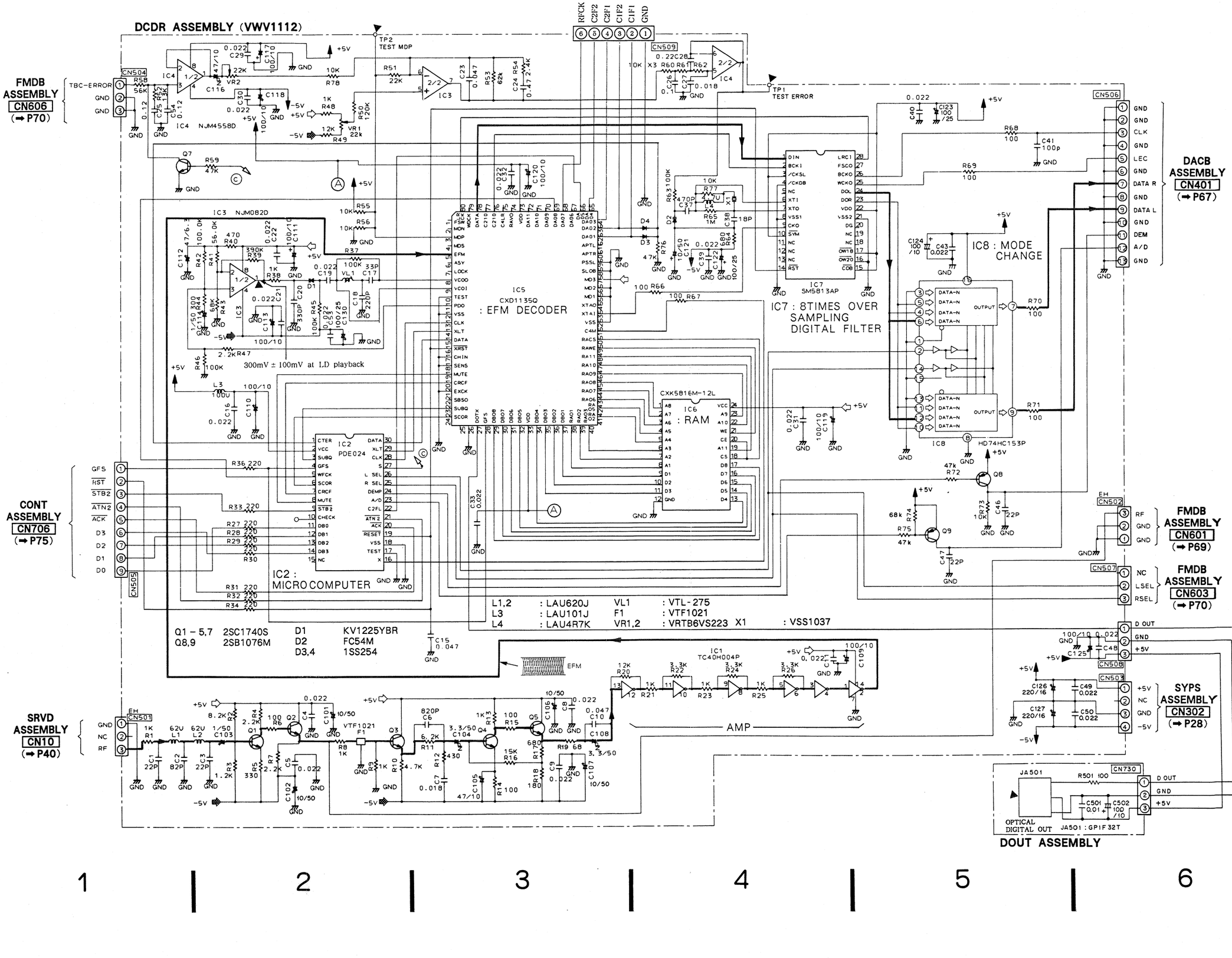


IC1,4	PA9003						
IC2,3	TC74HC4053AP						
Q1-3,6-9,11-20,22, Q23,25-28,31,34,38,40, Q81,201,203,205,207	2SC2412K	Q79,80	2SD2012	L201	: LAU6R8K		
Q4,10	2SC1583	Q208	2SC2412KLN	L202	: LAU470J		
Q5,21,210	DTC124EK	Q209	DTA124EK	L203	: LAU180J		
Q24,37,39,72,74,76	2SC1740S	Q211,212	DTA124ES	L204	: LAU270J		
Q29,32,33,35,36,202, Q204,206	2SA1037K	D1-6,71,72,74-79,90	1SS254	VR1	: VRTB6VS472		
Q30,71,73,75	2SA933S	D73,80	HZS5C1	VR2	: VRTG6VS102		
Q77,78	2SB1375	D81	SVC321SP	C48,49	: VCH1086		

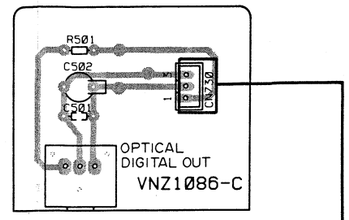
: Video Signal Line
: C Signal (CHR) Line
: Y Signal (CHR) Line

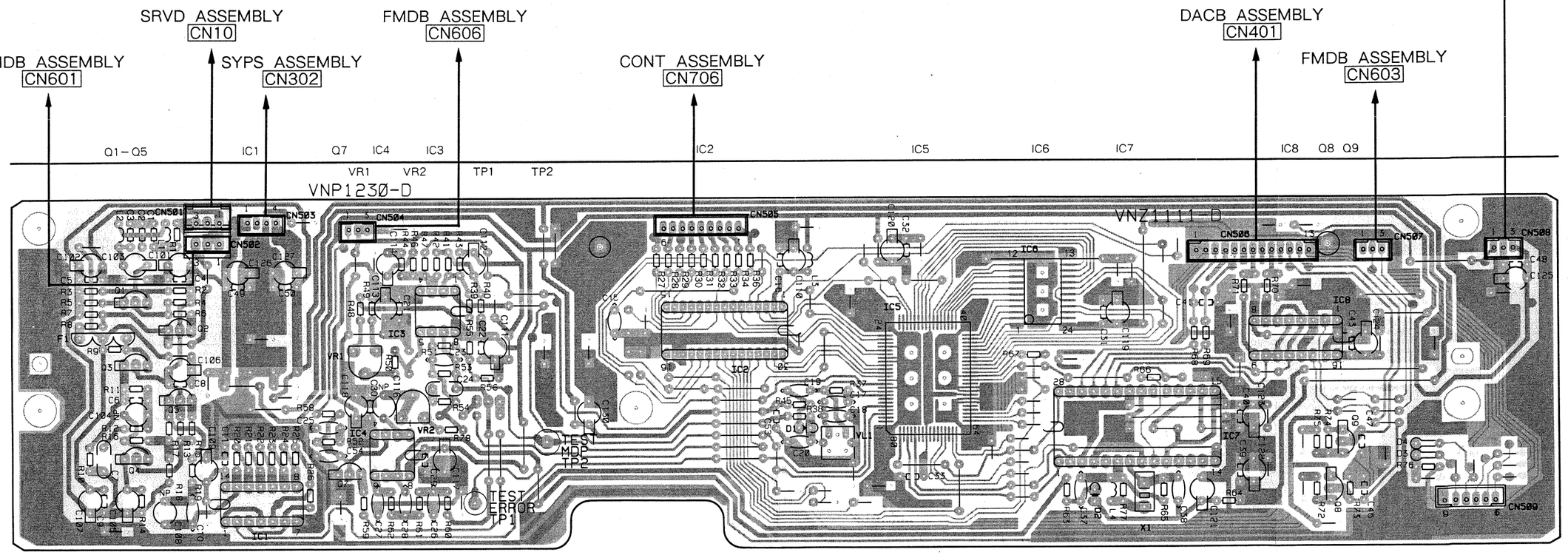
5.6 DCDR AND DOUT ASSEMBLIES

: RF Signal Line
: Digital Audio Signal Line



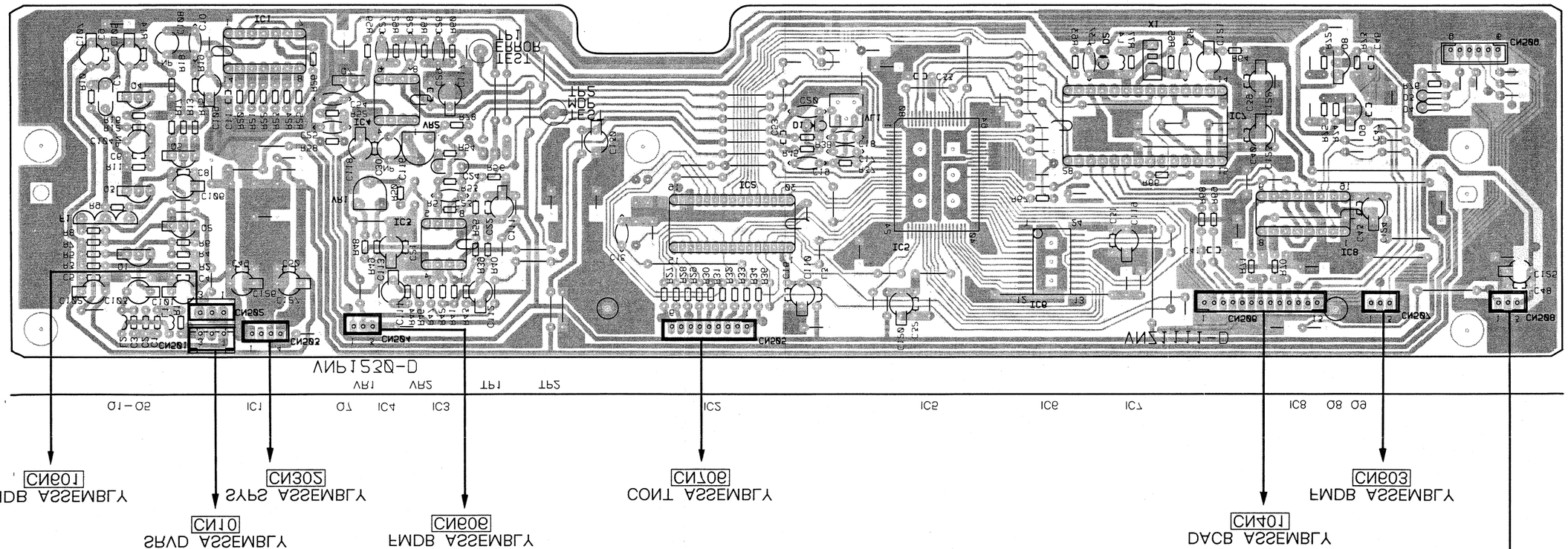
DOUT ASSEMBLY





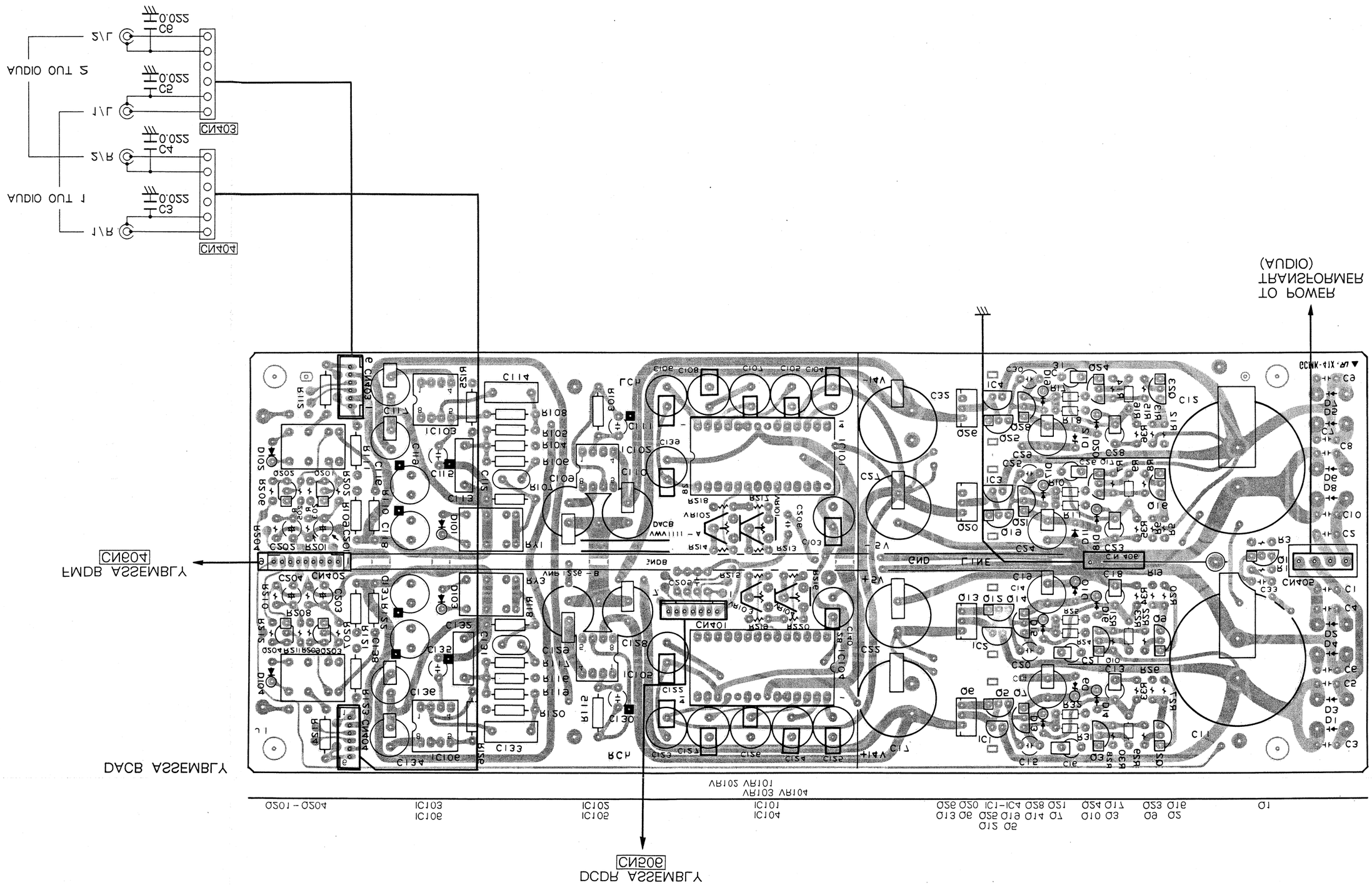
DCDR ASSEMBLY (VWV1112)

DCDR ASSEMBLY (VWV1111)

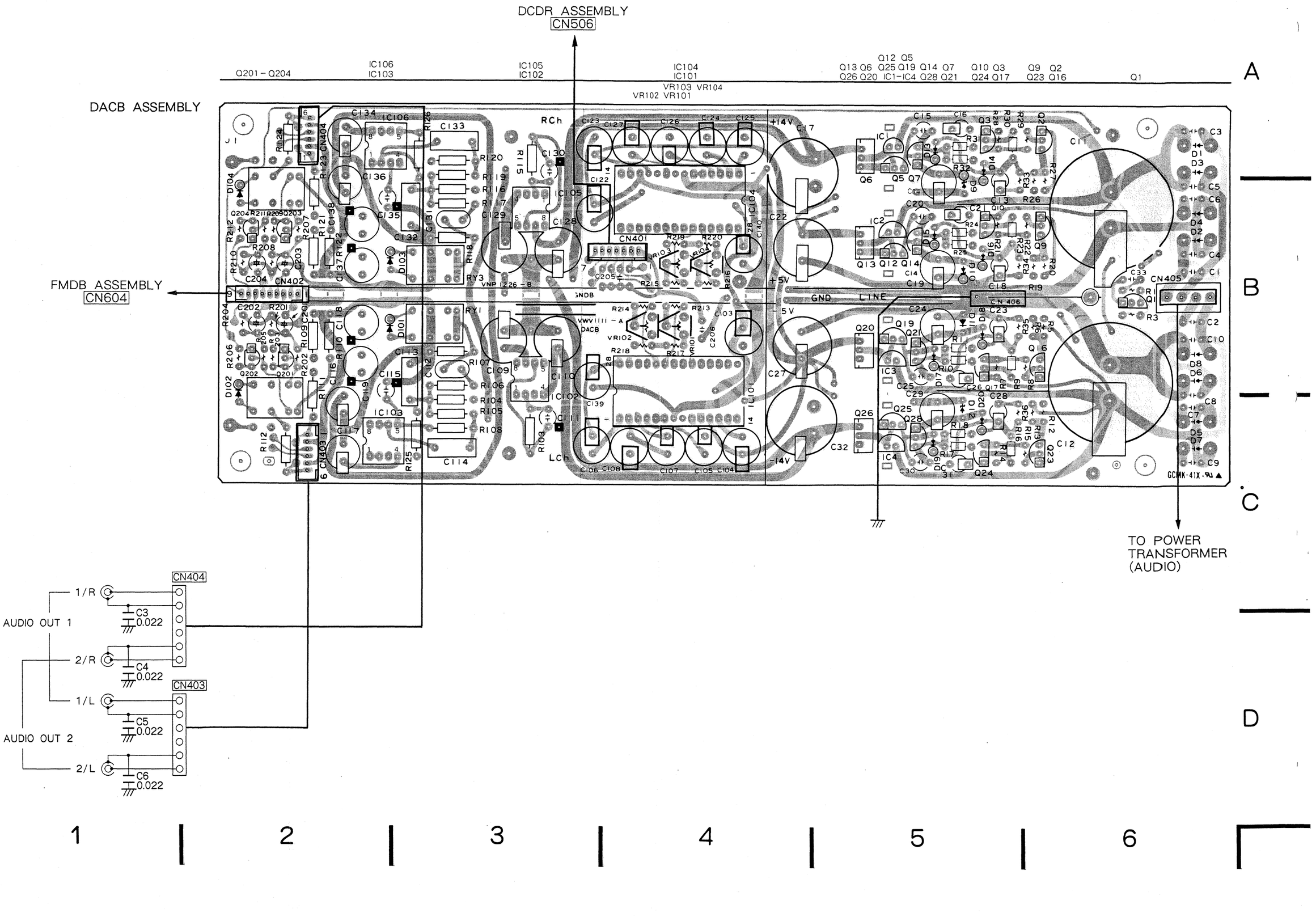


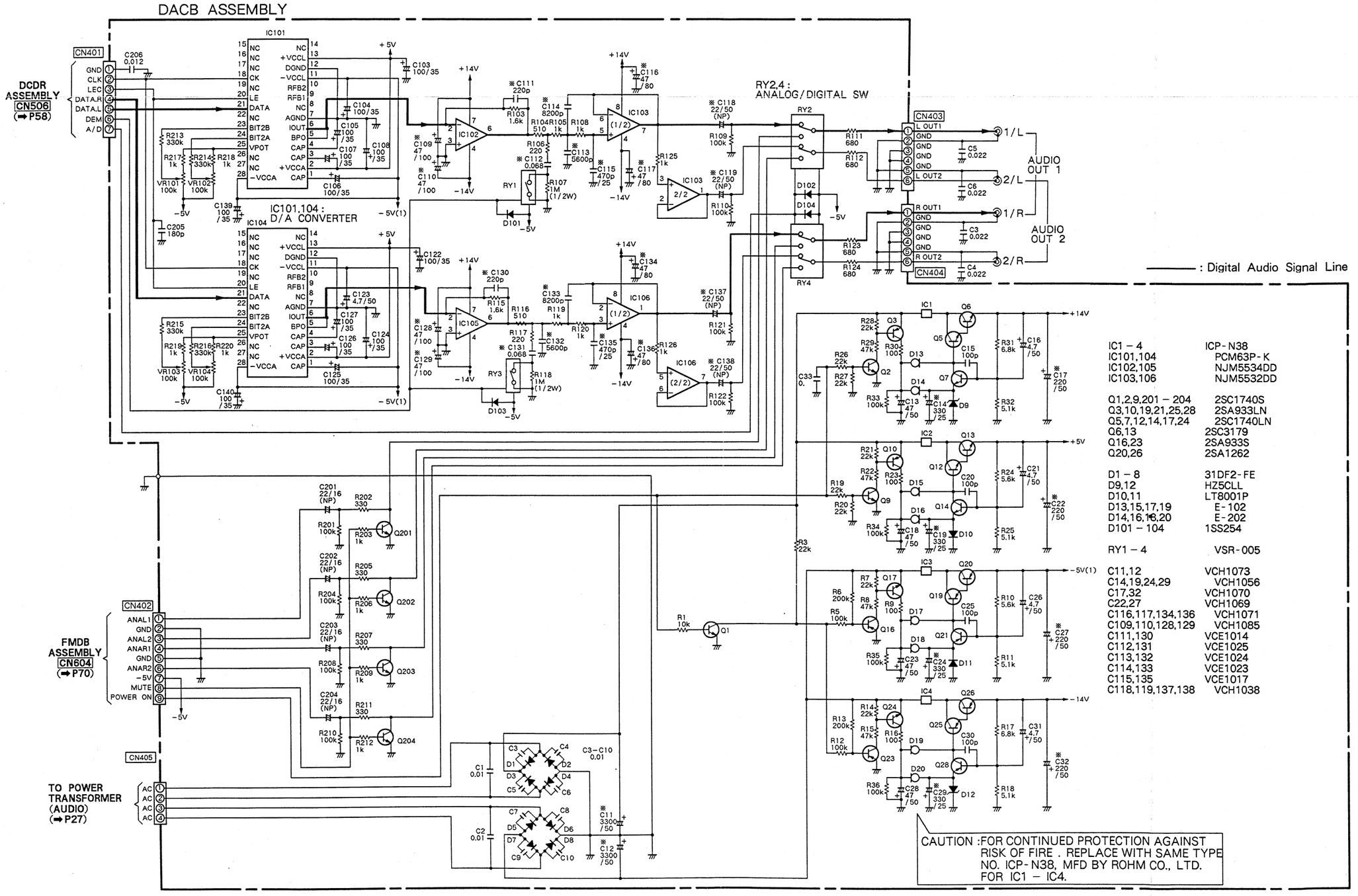
P.C.B. DACB AND SETB ASSEMBLIES

This P.C.B. connection diagram is viewed from the foil side.



5.7 DACB AND SETB ASSEMBLIES





IC1 – 4	ICP-N38
IC101,104	PCM63P-K
IC102,105	NJM5534DD
IC103,106	NJM5532DD
Q1,2,9,201 – 204	2SC1740S
Q3,10,19,21,25,28	2SA933LN
Q5,7,12,14,17,24	2SC1740LN
Q6,13	2SC3179
Q16,23	2SA933S
Q20,26	2SA1262
D1 – 8	31DF2-FE
D9,12	HZ5CLL
D10,11	LT8001P
D13,15,17,19	E-102
D14,16,18,20	E-202
D101 – 104	1SS254
RY1 – 4	VSR-005
C11,12	VCH1073
C14,19,24,29	VCH1056
C17,32	VCH1070
C22,27	VCH1069
C116,117,134,136	VCH1071
C109,110,128,129	VCH1085
C111,130	VCE1014
C112,131	VCE1025
C113,132	VCE1024
C114,133	VCE1023
C115,135	VCE1017
C118,119,137,138	VCH1038

5.8 FMDB ASSEMBLY

FMDB ASSEMBLY

: RF Signal Line
: Analog Audio Signal Line

IC101	PA0034A	L101	: LAU101J
IC102,103	BA15218N	L102	: LAU470J
IC104	NJM4558S	L103	: LAU560J
		F101	: RTF1084
Q101,102	2SC1740S		
Q103	DTA124ES		
Q104	DTC124ES		
D201–206	1SS254		

SYPS ASSEMBLY CN306 (➡P28)

DCDR ASSEMBLY CN502 (➡P58)

F101 : B.P.F

IC101 : ANALOG AUDIO DEMODULATION

CONT ASSEMBLY CN707 (➡P75)

DCDR ASSEMBLY CN504 (➡P57)

DACB ASSEMBLY CN402 (➡P67)

DCDR ASSEMBLY CN507 (➡P58)

This P.C.B. connection diagram is viewed from the foil side.

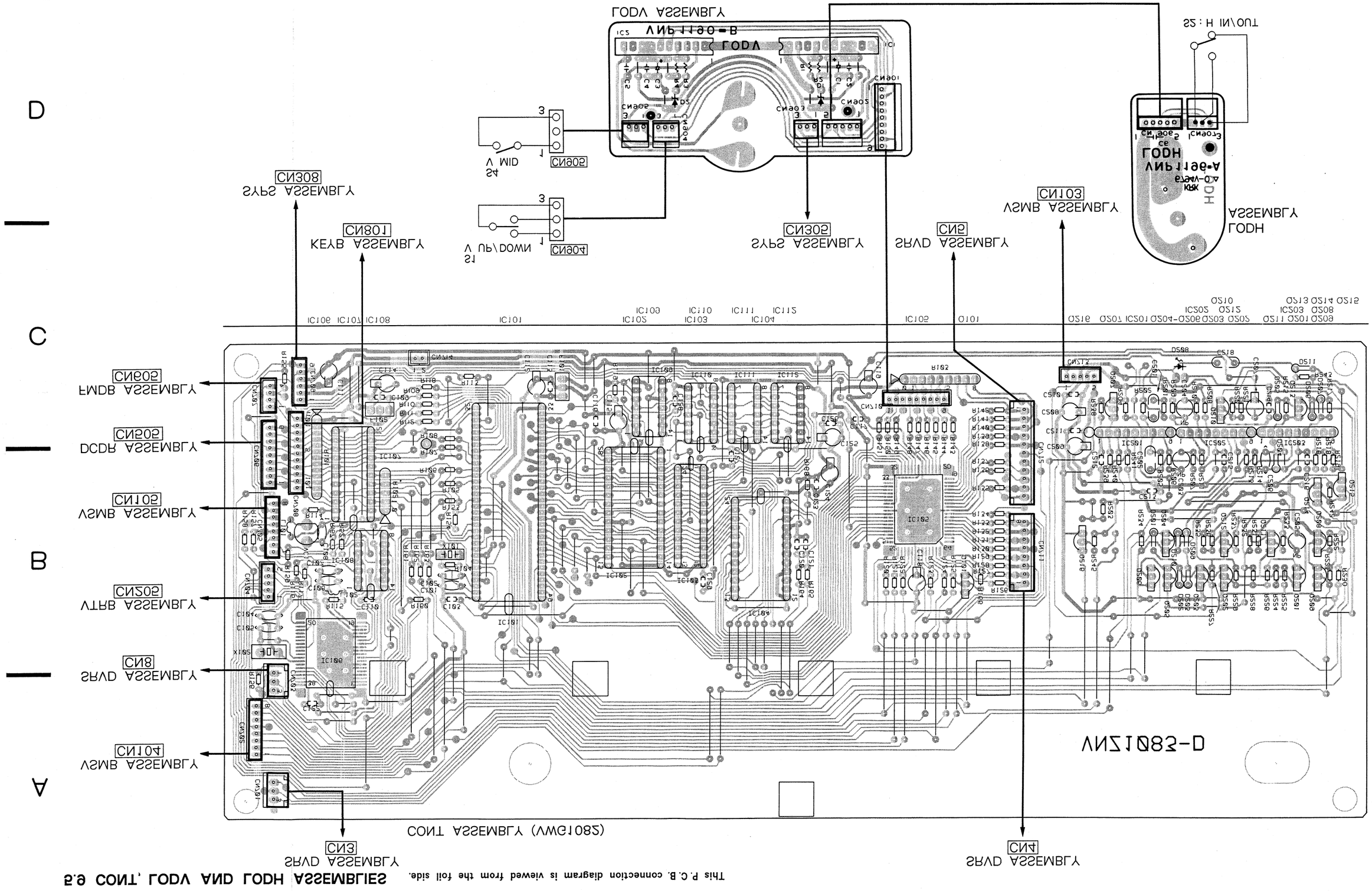
SYPS_ASSEMBLY CN306
DCDR_ASSEMBLY CN507
DCDR_ASSEMBLY CN504
DACB_ASSEMBLY CN402
DCDR_ASSEMBLY CN502
CONT_ASSEMBLY CN707
TO CASE

FMDB ASSEMBLY

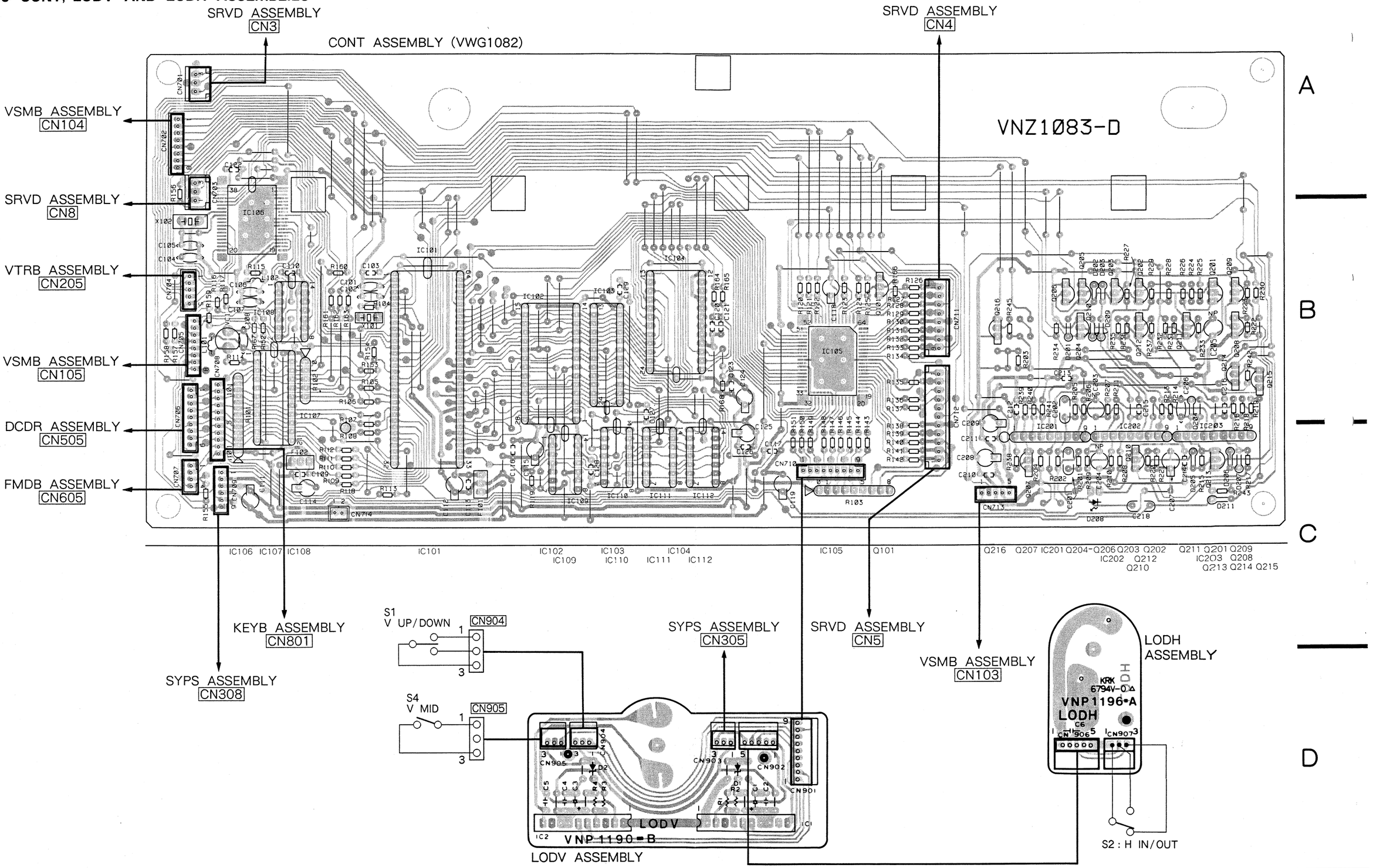
Q101 Q102 IC101 IC102 IC103 Q103 Q104 IC104

2.9 CONT, LOAV AND LOAH ASSEMBLIES

This P.C.B. connection diagram is viewed from the foil side.



5.9 CONT, LODV AND LODH ASSEMBLIES



CONT ASSEMBLY (VWG1082)

: SPDL Signal Line

VSMB ASSEMBLY CN103 (➡ P46)

SRVD ASSEMBLY CN8 (➡ P42)

FMDB ASSEMBLY CN605 (➡ P70)

DCDR ASSEMBLY CN505 (➡ P57)

KEYB ASSEMBLY CN801 (➡ P78)

SRVD ASSEMBLY CN3 (➡ P40)

SYPS ASSEMBLY CN308 (➡ P28)

LODV ASSEMBLY

IC1,2 TA7291P
D1 HZS7C1
D2 HZS9B3

LOADING MOTOR (V) ASSEMBLY VXX1352

SRVD ASSEMBLY CN5 (➡ P39)

SRVD ASSEMBLY CN4 (➡ P42)

VSMB ASSEMBLY CN104 (➡ P43)

SYPS ASSEMBLY CN305 (➡ P28)

LODH ASSEMBLY

LOADING MOTOR (H) ASSEMBLY VXX1358

IC101 : CPU

IC102 : ROM

IC103 : RAM

IC104 : UP / DOWN COUNTER

IC105 : EXPANSION I/O

IC106 : DISPLAY IC

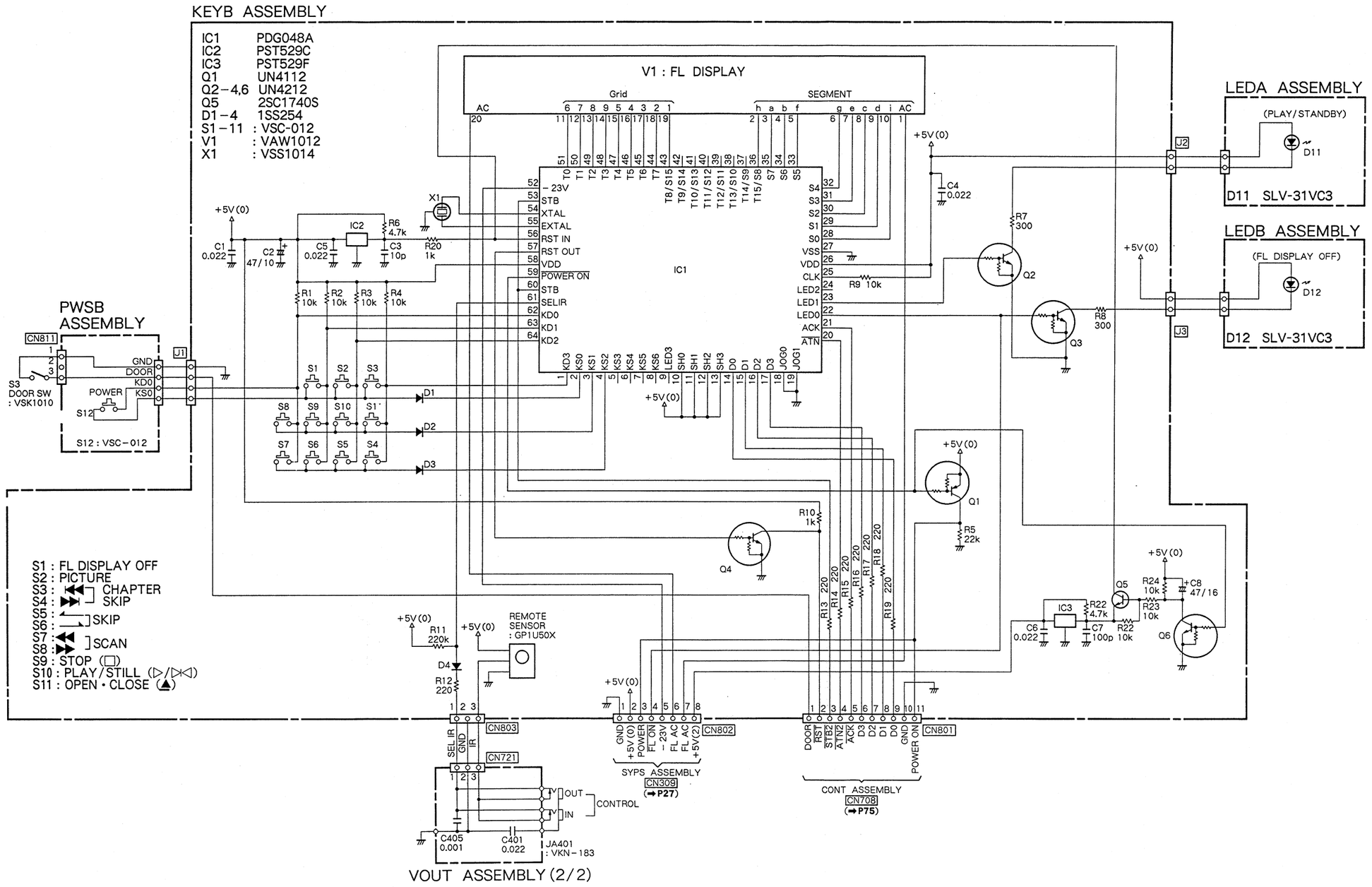
IC107 : DECODER 3MHz ± 100kHz

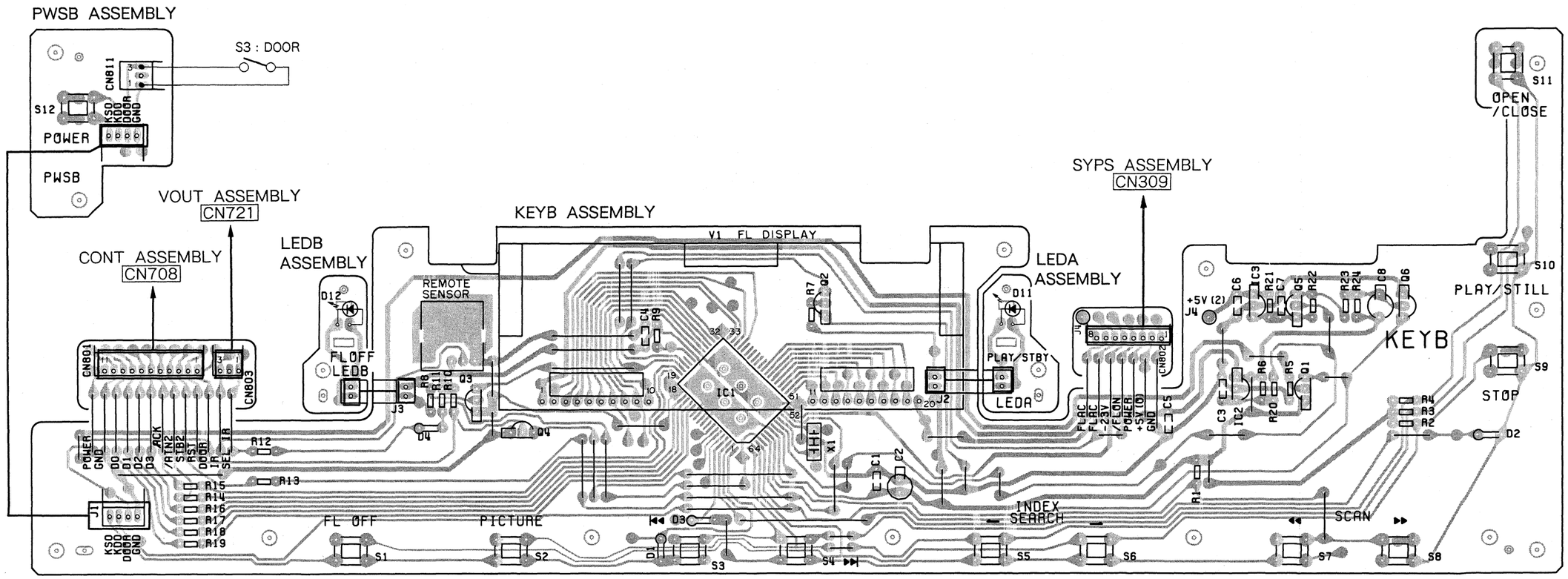
VSMB ASSEMBLY CN105 (➡ P43)

VTRB ASSEMBLY CN205 (➡ P55)

IC101	HD63B03YP	D201 – 207,211	1SS254
IC102	VYW1467	D208	SLV-31VC3
IC103	LC3517BSL-12	D209,210	HZS2B1
IC104	UPD4701AC		
IC105	CXD1095Q		
IC106	MB90061-101		
IC107	PD0011A	L101	: LAU221J
IC108 – 110	BU74HC00	L102	: LAU8R2J
IC111,112	MC74HC4078N	F101,102	: VTH1012
IC201 – 203	NJM4558S		
		VC1	: VCM-003
Q101,202–204,206, Q210,214 – 216	UN4112		
Q201,208,211,212	2SC1740S	R101	: VCN1017
Q205,207	UN4212	R102	: RA4S103J
Q209	2SA933S	R103	: RA8S472J
Q213	2SK184		
		X101	: KBR-8.0M
		X102	: VSS1029

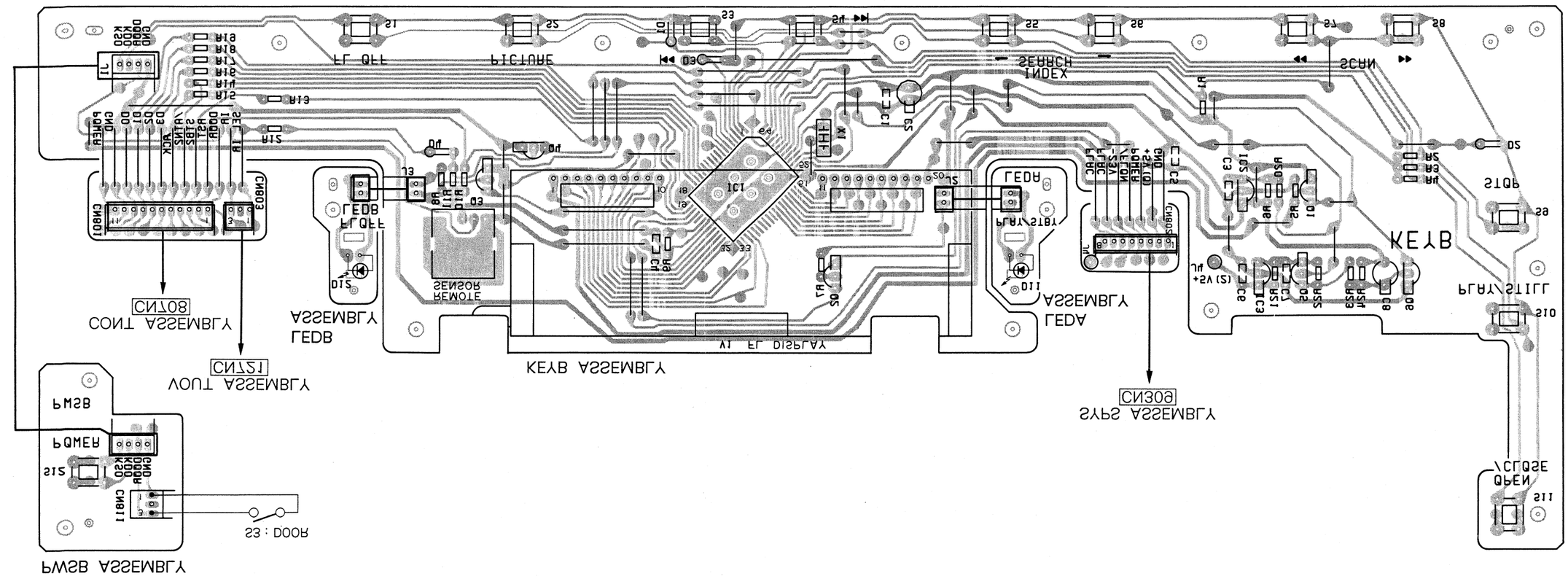
5.10 KEYB, LEDA, LEDB, PWSB AND VOUT (2/2) ASSEMBLY





FLKB VNP1232-A

Q3 Q4 IC1 Q2 IC2 IC3 Q5 Q1 Q6



This P. C.B. connection diagram is viewed from the foil side.

6. ELECTRICAL PARTS LIST

NOTES :
- Parts without part number cannot be supplied.
- Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.
- The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.
- When ordering resistors, first convert resistance values into code form as shown in the following examples.

Ex.1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J = 5 %, and K = 10 %).
560 Ω → 56 × 10^1 → 561 ····· RD1/4PS 5 6 1 J
47k Ω → 47 × 10^3 → 473 ····· RD1/4PS 4 7 3 J
0.5 Ω → 0R5 ····· RN2H 0 R 5 K
1 Ω → 010 ····· RS1P 0 1 0 K

Ex.2 When there are 3 effective digits (such as in high precision metal film resistors).
5.62k Ω → 562 × 10^1 → 5621 ····· RN1/4SR 5 6 2 1 F

Miscellaneous Parts

Mark	Symbol & Description	Part No.
	PWSB assembly	
	LODH assembly	
	LODV assembly	
◉	SRVD assembly	VWS1062
◉	DCDR assembly	VWV1112
	VOUT assembly	
◉	VSMB assembly	VWS1077
	KEYB assembly	
	FMDB assembly	
	DACB assembly	
◉	SYPS assembly	VWR1034
◉	VTRB assembly	VWV1093
	DOUT assembly	
◉	CONT assembly	VWG1082
	LSFB assembly	
	POSS assembly	
	LEDA assembly	
	LEDB assembly	
	Pickup assembly	VWY1020
⚠	FU5 Fuse (1A)	REK-080
⚠	FU1,FU2 Fuse (4A)	REK-084
⚠	FU3,FU4 Fuse (3A)	VEK-018
	IC102 Program P ROM-S (Install in the CONT assembly)	VYW1467
	S3 Slide switch (DOOR)	VSK1010
	S4 Micro switch (V MID)	VSF1001
	S6,S7 Slide switch (SLDR SHIP/REL)	VSK1009
	S5 Micro switch (TILT LIMIT)	VSF1005
	S1,S2 Lever switch (V. UP/DOWN, H. IN/OUT)	VSK1013
	C1 – C6	CKDYF223Z50
⚠	AC power cord	VDG1041
⚠	Power transformer (MAIN)	VTT1075
⚠	Power transformer (AUDIO)	VTT1076
	Spindle motor assembly	VXX1358
	Tilt motor assembly	VXX1359
	Loading motor (V) assembly	VXX1352
	Loading motor (H) assembly	VXX1353
	Remote control unit	VXX1370

PWSB Assembly

SWITCH

Mark	Symbol & Description	Part No.
	S12 Tact switch (POWER)	VSC-012

LODH Assembly

CAPACITOR

Mark	Symbol & Description	Part No.
	C6	CGDYX473M25

LODV Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC1,IC2	TA7291P
	D1	HZS7C1
	D2	HZS9B3

CAPACITORS

Mark	Symbol & Description	Part No.
	C1,C3	CEAS100M50
	C5	CGDYX473M25
	C2,C4	CKPUYY103N16

RESISTORS

Mark	Symbol & Description	Part No.
	All resistors	RD1/4VM□□□J

◉SRVD Assembly (VWS1062)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	TH1 Thermistor	D33A
	IC304	AN7810F
	IC12 – IC14	NJM072SH
	IC1,IC2	NJM082S
	IC9	NJM4556DE
	IC3 – IC8,IC10	NJM4558S
	IC301	PA0023
	IC302	PA3018
	IC303	PM0001
	IC11	PM4001
	IC15	TC4066BP
	Q18,Q20,Q21,Q24,Q25	UN4112
	Q9,Q11,Q308	UN4212
	Q1,Q309,Q319,Q323,Q328	2SA933S
	Q304,Q310	2SC1674
	Q23	2SB1065
	Q2 – Q4,Q10,Q12,Q15, Q301 – Q303,Q305 – Q307, Q311 – Q318,Q320 – Q322, Q325,Q327,Q329,Q330	2SC1740S
	Q7,Q14,Q17,Q326	2SB1185
	Q22	2SD1506
	Q6,Q13,Q16,Q324	2SD1762
	Q8	2SD973A
	Q5,Q19	2SK184
	D3,D4	HZS3B3
	D21,D22	1SR139-100
	D304,D312	HZS5C1
	D9,D13	MTZ5.6C
	D1,D2,D5 – D8,D10 – D12, D14 – D20,D301 – D303,D305, D307 – D309,D311,D313,D314	1SS254

COILS AND FILTERS

Mark	Symbol & Description		Part No.
	L311	Coil	VTL-011
	L312	(1.8μH)	VTL-014
	L302,L303	(12μH)	VTL-024
	L308	(22μH)	VTL-027
	L301	(30μH)	VTL1021
	L304,L305	(10μH)	VTL1022
	L306	(51μH)	VTL1023
	L309,L310	(390μH)	VTL-042
	L307	(47μH)	VTL1024
	F301,F302	EMI filter	VTH1012

CAPACITORS

Mark	Symbol & Description	Part No.
	C302	CCCCH020C50
	C303,C339	CCCCH060D50
	C326,C328,C356	CCCCH080D50
	C341	CCCCH030C50
	C304,C342	CCCCH120J50
	C353,C394	CCCCH121J50
	C357	CCCCH150J50
	C392	CCCCH180J50
	C361,C381,C382	CCCCH181J50
	C391	CCCCH220J50
	C338	CCCCH270J50
	C327,C340	CCCCH360J50
	C359	CCCCH390J50
	C329	CCCCH470J50
	C334,C397	CCCCH680J50
	C322,C323	CCCCH820J50
	C55	CCCSL151J50
	C34,C35	CCCSL221J50
	C324	CCCSL271J50
	C317,C360	CCCSL331J50
	C325	CCCSL391J50
	C66	CCCSL681J50
	C77	CEJANPR47M50
	C6 – C8,C18,C50,C64,C414	CEJANP010M50
	C30,C36,C413	CEJANP220M10
	C48,C60,C389	CEJANP3R3M25
	C61	CEJANP4R7M16
	C27,C393	CEJANP4R7M35
	C28,C31,C306,C308	CEJA010M50
	C32,C84,C309,C409,C410	CEJA100M16
	C76,C406	CEJA100M35
	C401,C405	CEJA101M6R3
	C23,C43,C46,C316,C363,C365, C369,C396	CEJA220M16
	C370	CEJA3R3M50
	C24,C25,C398,C402	CEJA330M25
	C78,C79,C345,C372,C399,C403, C408	CEJA470M16
	C319,C321,C331,C335,C337,C344, C349,C351,C362,C368,C375, C377-C379,C383,C384,C411, C412,C415,C416	CEJA470M6R3
	C63	CFTXA104J50
	C62	CFTXA683J50
	C68,C71	CFTXA823J50
	C17,C44,C47,C83,C301,C305,C307, C310,C312,C313,C315,C318,C320, C330,C336,C343,C346 – C348, C350,C352,C364,C371,C373,C374, C376,C380,C385,C388,C390,C400, C404,C407	CGCYX473M25
	C58,C332,C333,C358,C366,C386, C387	CKCYF103Z50
	C26,C67,C82,C311,C314,C395	CKCYF223Z50
	C39,C354,C355	CKPUYB102K50
	C1 – C5,C9 – C16,C21,C22,C33, C37,C42,C45,C49,C51,C52,C56, C57,C65,C70,C74,C80,C81	CKPUYF223Z25

Mark	Symbol & Description	Part No.
	C29,C40,C69	CQMA102J50
	C38	CQMA103J50
	C19	CQMA183J50
	C41	CQMA224J50
	C72	CQMA273J50
	C53	CQMA392J50
	C73	CQMA473J50
	C54	CQMA682J50
	C20,C59	CQMA822J50

RESISTORS

Mark	Symbol & Description	Part No.
	VR1 – VR3,VR9 Semi-fixed (10kΩ)	VRTB6VS103
	VR4 Semi-fixed (2.2kΩ)	VRTB6VS222
	VR5,VR6,VR8 Semi-fixed (4.7kΩ)	VRTB6VS472
	VR7 Semi-fixed (47kΩ)	VRTB6VS473
	VR303 Semi-fixed (1kΩ)	VRTG6VS102
	VR302 Semi-fixed (2.2kΩ)	VRTG6VS222
	VR301 Semi-fixed (470Ω)	VRTG6VS471
	R137	RS1PMF4R7J
	R81	RD1/4VM6R8J
	R201,R202	RD1/2PMF010J
	Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description	Part No.
	DL301 220nS delay line	VTF-063

◉DCDR Assembly (VWV1112)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC5	CXD1135Q
	IC6	CXK5816M-12L
	IC8	HD74HC153P
	IC3	NJM082D
	IC4	NJM4558D
	IC2	PDE024
	IC7	SM5813AP
	IC1	TC40H004P
	Q8,Q9	2SB1076M
	Q1 – Q5,Q7	2SC1740S
	D2	FC54M
	D1	KV1225YBR
	D3,D4	1SS254

COILS AND FILTER

Mark	Symbol & Description	Part No.
	L3	LAU101J
	L4	LAU4R7K
	L1,L2	LAU620J
	VL1 Variable coil	VTL-275
	F1 1.75MHz L.P.F	VTF1021

CAPACITORS

Mark	Symbol & Description	Part No.
	C38	CCCCH180J50
	C17	CCCCH330J50
	C18	CCCSL221J50
	C46,C47	CCPUSL220J50
	C1,C3	CCDCH220J50
	C41	CCCCH101J50
	C126,C127	CEYA221M16
	C121	CEYA100M50
	C104,C108	CEANP3R3M50
	C116	CEANP470M10
	C103,C114	CEAS010M50
	C101,C102,C106,C107	CEAS100M50
	C109 – C111,C113,C117 – C120, C124,C125	CEAS101M10
	C122,C123,C130	CEYA101M25
	C105,C112	CEAS470M10
	C26	CFTXA104J50
	C25,C54	CFTXA124J50
	C7,C27	CFTXA183J50
	C28	CFTXA224J50
	C23	CFTXA473J50
	C24	CFTXA474J50
	C19	CGCYX223K25
	C10,C15	CGCYX473K25
	C20	CCCSL331J50
	C37	CCCSL471J50
	C2	CCDCH820J50
	C6	CQSH821J50
	C4,C5,C8,C9,C11,C16,C21,C22, C29 – C33,C39,C40,C43, C48 – C50,C53	CKPUYF223Z25

RESISTORS

Mark	Symbol & Description	Part No.
	VR1,VR2 Semi-fixed (22kΩ)	VRTB6VS223
	R41,R42	RN1/6PQ□□□□F
	Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description	Part No.
	X1 Crystal resonator	VSS1037

VOUT Assembly

CAPACITORS

Mark	Symbol & Description	Part No.
	C401,C402	CKCYF223Z50
	C404	CKPUYF223Z25
	C405	CKCYB102K50

OTHERS

Mark	Symbol & Description	Part No.
	JA401 2P mini jack	VKN-183
	4P mini DIN socket	VKN1078

◉ VSMB Assembly (VWS1077)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC2	HA19211NT
	IC19	HM53051P-45
	IC12	HM63021P-34
	IC20,IC21	MB40778
	IC9,IC10	MN4700
	IC8	MN4760S
	IC3	NJM082D
	IC4	NJM4558D
	IC6	PA0009
	IC1	PA5012
	IC7	PDB005
	IC11	PDB006
	IC18	PDB009
	IC13	PD5087
	IC5	TC74HCU04AP
	IC16	TC74HC00AP
	IC17	TC74HC164AP
	IC23	TC74HC4053AP
	IC15	TC74HC74AP
	IC14	TC9015P
	Q11,Q12	DTA124ES
	Q1	UN4212
	Q16,Q18,Q22,Q24	2SA1037K
	Q2,Q3,Q14	2SA933S
	Q13	2SC1740S
	Q4 – Q10,Q15,Q17,Q19 – Q21, Q23,Q25 – Q27	2SC2412K
	D6	HZS2C2
	D1,D2,D4,D5,D7	1SS254
	D3	1SV68

COILS AND FILTERS

Mark	Symbol & Description	Part No.
	VL1 Variable coil	VTL1012
	L5 – L9,L11,L12,L22,L23	LAU100J
	L4	LAU120J
	L2	LAU121J
	L18,L21	LAU150J
	L3	LAU181J
	L25	LAU4R7K
	L24	LAU6R8K
	L16,L17,L19,L20	LAU220J
	L1	LAU270J
	L101 Ferrite bead	VTH1013
	F1,F5 – F8 EMI filter	VTH1018

CAPACITORS

Mark	Symbol & Description	Part No.
	VC1 Ceramic trimmer (45p)	VCM1002
	C30	CCCCH200J50
	C118	CCCSL151J50
	C105	CCCCH180J50
	C103,C116	CCPUCH150J50
	C83,C85,C147,C149,C156,C157	CEAS471M10
	C64	CCPUCH100J50
	C101,C114	CCPUCH5R6K50
	C3,C6,C8,C28,C56	CCSQCH101J50
	C32,C165	CCSQCH150J50
	C68,C72	CCSQCH151J50
	C31,C43,C45,C113,C142,C163	CCSQCH220J50
	C11,C51	CCSQCH271J50
	C33,C65	CCSQCH330J50
	C50,C104,C117	CCSQCH470J50
	C158	CCSQCH180J50
	C107,C120	CCSQCH390J50
	C102,C115	CCSQCH560J50
	C7,C71,C164	CCSQCH680J50
	C59,C60	CCSQSL331J50
	C9,C55,C58	CCSQSL681J50
	C4,C54	CEALNPR47M50
	C125	CEALNP010M50
	C19	CEALNP220M16
	C112	CEALNP330M10
	C106,C119,C143	CEALNP470M6R3
	C48,C90,C96	CEAL010M50
	C160,C161	CEAL100M16
	C36 – C39	CEAL100M50
	C74	CEAL101M6R3
	C61,C100	CEAL220M16
	C91,C97	CEAL220M6R3
	C49	CEAL470M16
	C2,C16,C18,C21,C23,C26,C35, C42,C47,C63,C75,C78,C88, C95,C99,C108,C110,C121,C123, C132,C134,C139	CEAL470M6R3
	C159	CKSQYB822K50
	C137	CFTXA103J50
	C25,C67	CFTXA104J50
	C24,C52,C53	CFTXA153J50
	C57	CFTXA823J50
	C140	CKPUYF103Z25
	C66	CKSQYB472K50
	C1,C17,C20,C22,C27,C34,C41,C46, C62,C73,C76,C77,C79 – C82,C84, C87,C89,C93,C94,C98,C109,C111, C122,C124,C133,C135,C136,C138, C141,C144,C145,C148,C154,C155	CKSQYF104Z25
	C15,C29,C40,C44,C146	CKSQYF103Z50
	C5	CQMA102J50
	C14	CQMA122J50
	C10	CQMA332J50
	C13	CQMA682J50
	C12 (150p)	VCE1022

RESISTORS

Mark	Symbol & Description	Part No.
	VR5 Semi-fixed (1kΩ)	VRTB6VS102
	VR1,VR2,VR4 Semi-fixed (10kΩ)	VRTB6VS103
	VR3 Semi-fixed (22kΩ)	VRTB6VS223
	VR7 – VR9 Semi-fixed (4.7kΩ)	VRTG6VS472
	R189,R190 Resistor array	RA4S332J
	R73 – R81,R92,R93, R96,R144,R145	RD1/6PM□□□J
	Other resistors	RS1/10S□□□J

OTHERS

Mark	Symbol & Description	Part No.
	X1 Crystal (14.318MHz)	VSS1029

KEYB Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC1	PDG048A
	IC2	PST529C
	IC3	PST529F
	Q1	UN4112
	Q2 – Q4,Q6	UN4212
	Q5	2SC1740S
	D1 – D4	1SS254

SWITCHES

Mark	Symbol & Description	Part No.
	S1 – S11 Tact switch (FL DISPLAY OFF, PICTURE, CHAPTER, SKIP (⏮,⏭), INDEX SKIP (→, ←), SCAN (◀◀,▶▶), STOP, PLAY/STILL, OPEN • CLOSE)	VSC-012

CAPACITORS

Mark	Symbol & Description	Part No.
	C2	CEAL470M10
	C3,C7	CKPUYB101K50
	C1,C4,C5,C6	CKPUYF223Z25
	C8	CEAL470M16

RESISTORS

Mark	Symbol & Description	Part No.
	All resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description	Part No.
	V1 FL display	VAW1012
	X1 Ceramic resonator	VSS1014
	Remote control sensor	GP1U50X

FMDB Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC102,IC103	BA15218N
	IC104	NJM4558S
	IC101	PA0034A
	Q103	DTA124ES
	Q104	DTC124ES
	Q101,Q102	2SC1740S
	D201 – D206	1SS254

COILS AND FILTER

Mark	Symbol & Description	Part No.
	L101	LAU101J
	L102	LAU470J
	L103	LAU560J
	F101 B,P,F 2.30, 2.81MHz	RTF1084

CAPACITORS

Mark	Symbol & Description	Part No.
	C202	CCCCH131J50
	C214	CCCSL271J50
	C215	CCCSL301J50
	C238	CCPUSL220J50
	C201	CCPUSL390J50
	C216,C217	CCPUSL560J50
	C311,C312	CEANP220M10
	C321	CEANP330M10
	C313	CEASR47M50
	C318	CEAS010M50
	C301,C302,C314	CEAS100M50
	C307,C308	CEAS101M25
	C309,C310,C316,C317	CEAS220M25
	C303 – C306,C315,C319,C320, C322 – C327	CEAS221M10
	C226	CFTXA104J50
	C234	CFTXA474J50
	C235	CFTXA564J50
	C203	CKPUYB910K50
	C204,C205,C210 – C213	CKPUYY103M16
	C206 – C209,C227 – C233,C239, C240	CKPUYY103N16
	C224,C225	CQMA393J50
	C220 – C223	CQMA472J50
	C218,C219	CQMA682J50

RESISTORS

Mark	Symbol & Description	Part No.
	All resistors	RD1/6PM□□□J

DACB Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC1 – IC4	ICP-N38
	IC103,IC106	NJM5532DD
	IC102,IC105	NJM5534DD
	IC101,IC104	PCM63P-K
	Q20,Q26	2SA1262
	Q3,Q10,Q19,Q21,Q25,Q28	2SA933LN
	Q16,Q23	2SA933S
	Q5,Q7,Q12,Q14,Q17,Q24	2SC1740LN
	Q1,Q2,Q9,Q201 – Q204	2SC1740S
	Q6,Q13	2SC3179
	D13,D15,D17,D19	E-102
	D14,D16,D18,D20	E-202
	D9,D12	HZ5CLL
	D101 – D104	1SS254
	D1 – D8	31DF2-FE
	D10,D11	LT8001P

RELAYS

Mark	Symbol & Description	Part No.
	RY1 – RY4 Relay	VSR-005

CAPACITORS

Mark	Symbol & Description	Part No.
	C201 – C204	CEANP220M16
	C103 – C108,C122 – C127,C139, C140	CENA101M35
	C16,C21,C26,C31	CENA4R7M50
	C13,C18,C23,C28	CENA470M50
	C1 – C10,C33	CKCYF103Z50
	C205	CCDCH181J50
	C15,C20,C25,C30	CQSF101J125
	C206	CFTXA123J50
	C114,C133 (8200p)	VCE1023
	C113,C132 (5600p)	VCE1024
	C112,C131 (0.068μ)	VCE1025
	C118,C119,C137,C138 (22μ/50V)	VCH1038
	C14,C19,C24,C29 (330μ/25V)	VCH1056
	C22,C27 (220μ/50V)	VCH1069
	C17,C32 (220μ/50V)	VCH1070
	C116,C117,C134,C136 (47μ/80V)	VCH1071
	C109,C110,C128,C129 (47μ/100)	VCH1085
	C11,C12 (3300μ/50V)	VCH1073
	C111,C130 (220p)	VCE1014
	C115,C135 (470p/25V)	VCE1017

RESISTORS

Mark	Symbol & Description	Part No.
	VR101 – VR104	VRTB6VS104
	R103 – R112,R115 – R126	RDM1/2P□□□J
	R9,R16,R23,R30	RDR1/2PM101J
	R10,R11,R17,R18,R24,R25, R31,R32	RDR1/4PM□□□J
	Other resistors	RD1/6PM□□□J

◉SYPS Assembly (VWR1034)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC2,IC3	ICP-N20
	IC1	NJM4558S
	Q14	UN4112
	Q21	UN4212
	Q2,Q4,Q9,Q17	2SA933S
	Q1,Q23	2SB1375
	Q22	2SB793A
	Q16,Q19	2SC1627
	Q3,Q5,Q10 – Q13,Q15,Q18	2SC1740S
	Q20	2SD1267
	Q6 – Q8	2SD2012
	D1,D2	D3SBA20
	D30	HZS24NB3
	D5,D13	HZS5C1
	D16,D22	HZS5C2
	D23	S2K20
	D24 – D29	1SR139-100
	D3,D4,D6 – D9,D11,D12,D14, D15,D17,D18,D21,D31 – D33	1SS254

RELAYS AND FUSE

Mark	Symbol & Description	Part No.
	RY2 Relay	VSR-005
	RY1 Relay	VSR1005
⚠	FU6 Fuse (1A)	VEK1001

COILS

Mark	Symbol & Description	Part No.
	L2,L3	LAU010K
	L1 Choke coil	VTT1016

CAPACITORS

Mark	Symbol & Description	Part No.
	C10,C13,C16,C17	CEAS101M10
	C31,C32	CEAS101M50
	C29	CEAS222M25
	C26	CEAS3R3M50
	C9,C12,C14,C15	CEAS470M16
	C28,C37	CEAS470M50
	C8 Elect. (6800μ/16V)	VCH1053
	C20,C30	CEJA100M50
	C23	CKPUYB102K50
	C21	CQMA332J50
	C27	CKPUYB471K50
	C1 – C4,C24,C25,C33 – C36, C38,C39	CKPUYF223Z25
	C22	CQMA183J50
	C7 Elect. (2200μ/16V)	VCH1074
	C5,C6 Elect. (6800μ/25V)	VCH1075

RESISTORS

Mark	Symbol & Description	Part No.
	R31,R32	RS1LMF□□□J
	R29,R30,R37,R38	RN1/6PQ□□□□F
	Other resistors	RD1/6PM□□□J

◉ VTRB Assembly (VWV1093)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC1,IC4	PA9003
	IC2,IC3	TC74HC4053AP
	Q5,Q21,Q210	DTC124EK
	Q29,Q32,Q33,Q35,Q36,Q202, Q204,Q206	2SA1037K
	Q30,Q71,Q73,Q75	2SA933S
	Q77,Q78	2SB1375
	Q4,Q10	2SC1583
	Q24,Q37,Q39,Q72,Q74,Q76	2SC1740S
	Q211,Q212	DTA124ES
	Q208	2SC2412KLN
	Q1 – Q3,Q6 – Q9,Q11 – Q20,Q22, Q23,Q25 – Q28,Q31,Q34,Q38,Q40, Q81,Q201,Q203,Q205,Q207	2SC2412K
	Q79,Q80	2SD2012
	Q209	DTA124EK
	D73,D80	HZS5C1
	D81	SVC321SP
	D1 – D6,D71,D72,D74 – D79,D90	1SS254

COILS

Mark	Symbol & Description	Part No.
	L203	LAU180J
	L204	LAU270J
	L202	LAU470J
	L201	LAU6R8K

CAPACITORS

Mark	Symbol & Description	Part No.
	C48,C49	VCH1086
	C209,C210	CCCCH070D50
	C6	CCCCH080J50
	C212	CCCCH120J50
	C7	CCCCH150J50
	C207,C211,C213	CCCCH390J50
	C20,C35	CCCSL101J50
	C1	CCCSL161J50
	C9,C10	CCCSL181J50
	C21,C36	CCCSL201J50
	C16,C27	CCCSL331J50
	C28	CEANPR47M50
	C23,C208	CEANP010M50
	C3,C11,C29	CEANP100M16
	C14	CEANP101M6R3
	C2	CCCSL221J50
	C219	CEALNPR47M50
	C218	CFTXA393J50
	C220,C221	CEAS470M25
	C54	CEANP220M16
	C38	CEANP470M10
	C37,C201	CEANP470M16
	C41,C45	CEAS100M16
	C15,C18,C25,C26,C30,C42,C43, C47,C50 – C52,C59,C74,C85, C86,C87,C89,C216,C217	CEAS101M10
	C202,C205	CEAS470M16
	C71 – C73,C75 – C79,C84	CEHAQ101M10
	C80	CEHAQ331M6R3
	C203	CFTXA102J50
	C218	CFTXA393J50
	C8	CFTXA392J50
	C206	CKCYB222K50
	C12,C13	CKCYF103Z50
	C4,C5,C17,C22,C24,C33,C53	CKSQYF103Z50
	C55,C56,C61,C81,C204,C214,C215	CKSQYF104Z25
	C34,C57,C58,C60,C82,C83	CKSQYF223Z50
	C19	CQMA512J50

RESISTORS

Mark	Symbol & Description	Part No.
	VR1 Semi-fixed (4.7kΩ)	VRTB6VS472
	VR2 Semi-fixed (1kΩ)	VRTG6VS102
	R1,R2,R13,R24,R27,R28,R42,R45, R46,R63 – R66,R77,R80,R93,R95, R98 – R100,R102 – R106, R108 – R117,R119,R120, R123,R124,R201,R203 – R205, R215,R220,R225,R226, R300 – R307,R310,R311	RD1/6PM□□□J
	R95,R102,R105,R109,R124	RN1/6PQ□□□□F
	Other resistors	RS1/10S□□□J

DOUT Assembly

CAPACITORS

Mark	Symbol & Description	Part No.
	C502	CEAS101M10
	C501	CKPUYY103N16

RESISTOR

Mark	Symbol & Description	Part No.
	R501	RD1/6PM101J

OTHERS

Mark	Symbol & Description	Part No.
	JA501 Optical transmit module (Optical digital output)	GP1F32T

◉CONT Assembly (VWG1082)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC108 – IC110	BU74HC00
	IC105	CXD1095Q
	IC101	HD63B03YP
	IC103	LC3517BSL-12
	IC106	MB90061-101
	IC111,IC112	MC74HC4078N
	IC201 – IC203	NJM4558S
	IC107	PD0011A
	IC104	UPD4701AC
	Q101,Q202 – Q204,Q206,Q210, Q214 – Q216	UN4112
	Q205,Q207	UN4212
	Q209	2SA933S
	Q201,Q208,Q211,Q212	2SC1740S
	Q213	2SK184
	D209,D210	HZS2B1
	D208	SLV-31VC3
	D201 – D207,D211	1SS254

COILS AND FILTERS

Mark	Symbol & Description	Part No.
	L101	LAU221J
	L102	LAU8R2J
	F101,F102 EMI filter	VTH1012

CAPACITORS

Mark	Symbol & Description	Part No.
	VC1 Ceramic trimmer	VCM-003
	C206	CCCCH101J50
	C104	CCCCH150J50
	C107	CCCCH180J50
	C102,C106,C108	CCCCH220J50
	C101	CCCCH330J50
	C105	CCCCH390J50
	C120,C121	CCPUSL680J50
	C203	CEJANPR47M50
	C204,C205	CEJANP4R7M16
	C111,C112,C114,C115,C118,C124, C125,C208,C209	CEJA101M6R3
	C119,C207	CEJA220M35
	C201	CFTXA104J50
	C202	CFTXA823J50
	C103,C109,C110,C113,C116,C117, C122,C123,C126 – C129, C210 – C216	CKPUYY103N16
	C218	CFTXA103J50

RESISTORS

Mark	Symbol & Description	Part No.
	R101 Resistor array (10kΩ × 12)	VCN1017
	R102 Resistor array (10kΩ × 4)	RA4S103J
	R103 Resistor array (4.7kΩ × 8)	RA8S472J
	R203,R204,R245	RN1/6PQ□□□□F
	Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description	Part No.
	X101 Ceramic resonator	KBR-8.0M
	X102 Crystal (14.318MHz)	VSS1029
	28 pin IC socket	VKH1001

LSFB Assembly

CAPACITORS

Mark	Symbol & Description	Part No.
⚠	C301,C302 (0.01μ/AC250V)	RCG-009

FILTER

Mark	Symbol & Description	Part No.
⚠	L301 Line filter	VTL-157

POSS Assembly

SEMICONDUCTOR

Mark	Symbol & Description	Part No.
	IC501	GP1A30R

CAPACITOR

Mark	Symbol & Description	Part No.
	C501	CKPUYF223Z25

RESISTOR

Mark	Symbol & Description	Part No.
	R501	RD1/6PM121J

LEDA Assembly

SEMICONDUCTOR

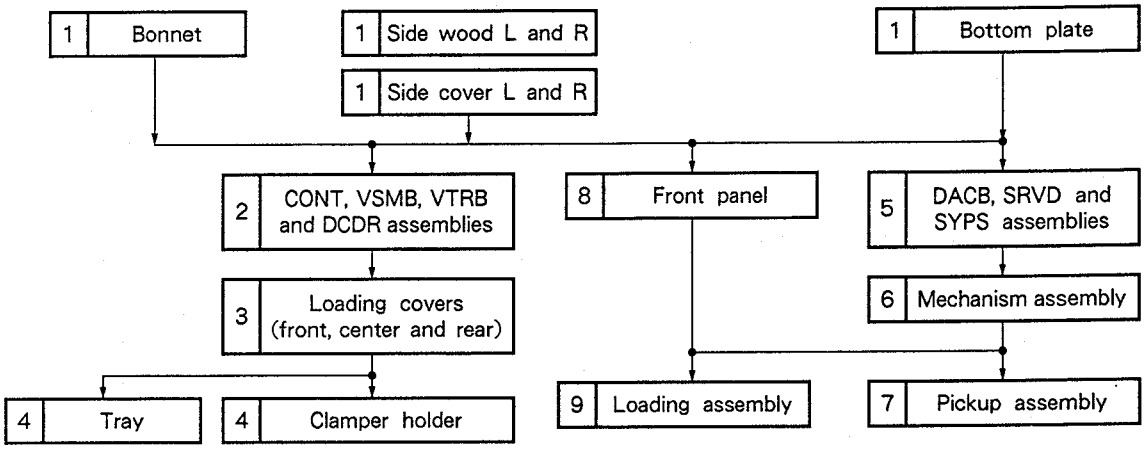
Mark	Symbol & Description	Part No.
	D11	SLV-31VC3

LEDB Assembly

SEMICONDUCTOR

Mark	Symbol & Description	Part No.
	D12	SLV-31VC3

7. DISASSEMBLY



1. Removing the bonnet, side wood L and R, bottom plate and side cover L and R

① Remove six screws Ⓐ from the bonnet .
② Remove eight screws Ⓑ from the left and right side woods.
③ Remove three screws Ⓒ at the rear of the bonnet.
④ Remove eight screws Ⓓ from the bottom plate.
⑤ Remove twelve screws Ⓔ from the left and right side covers.

Note: In the tray-out position, insert the philips head screw to the hole in the direction of arrow (Fig. 7-1), then disc tray is able to removed by loosen three tray-stopper screws.

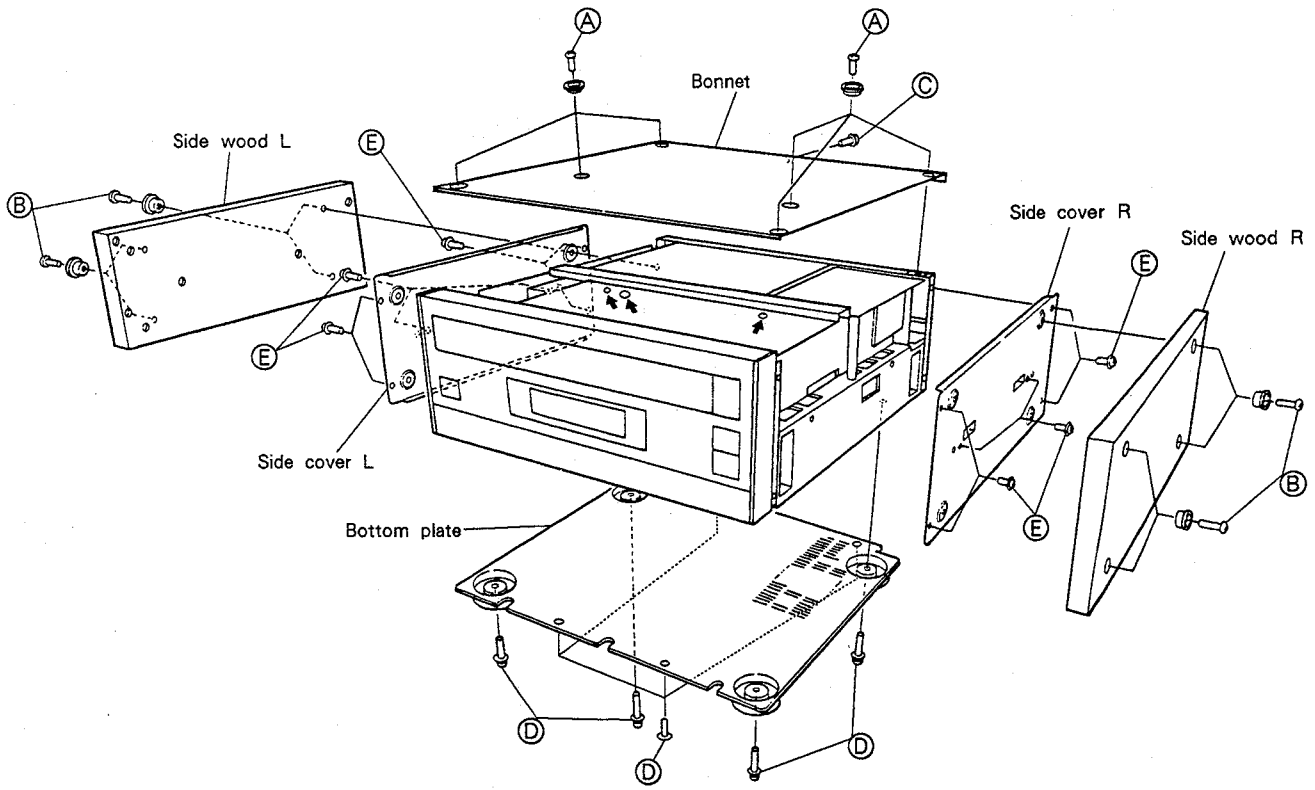


Fig. 7-1 Removing the bonnet, side wood L, R, bottom plate, side cover L and R

2. Removing the CONT, VSMB, VTRB and DCDR assemblies

① Remove four screws Ⓐ from the CONT assembly.
② Remove four screws Ⓑ from the VSMB assembly.
③ Remove four screws Ⓒ from the VTRB assembly.
④ Remove two screws Ⓓ from the bridge (A).
⑤ Remove five screws Ⓔ from the DCDR assembly.

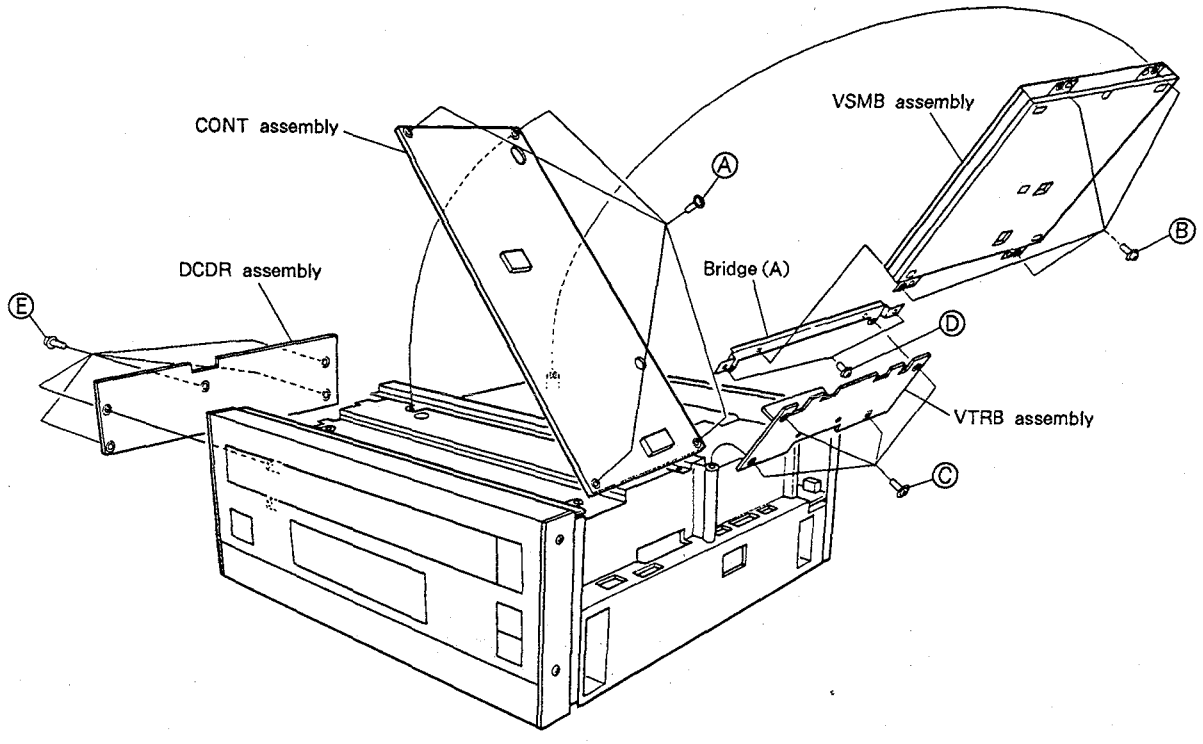


Fig. 7-2 Removing the CONT, VSMB, VTRB and DCDR assemblies

3. Removing the loading covers (front, center and rear)

① Remove four screws Ⓐ from the front.
② Remove two screws Ⓑ from the center.
③ Remove four screws Ⓒ from the rear.

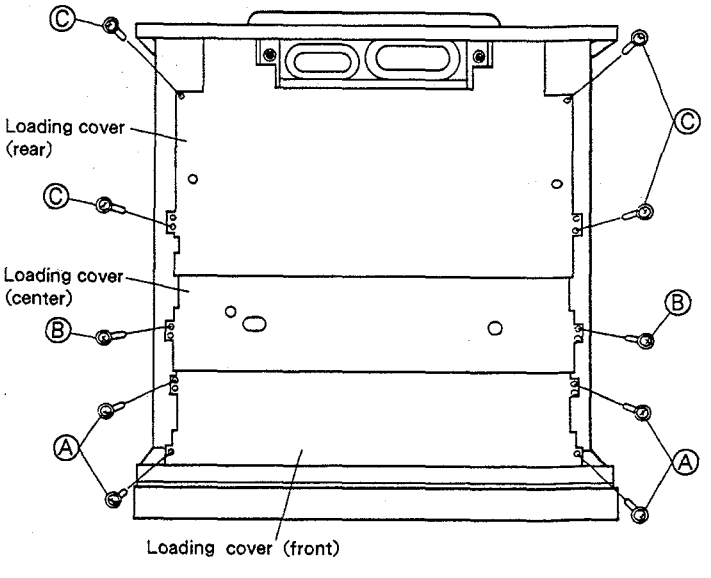


Fig. 7-3 Removing the loading covers (front, center and rear)

4. Removing the tray and clamper holder

① Remove four screws Ⓐ from the clamper holder.
② Insert the screwdriver into the guide L assembly and push out the rack L.
③ Remove three screws Ⓑ from the tray.
④ Pull the tray straight out.

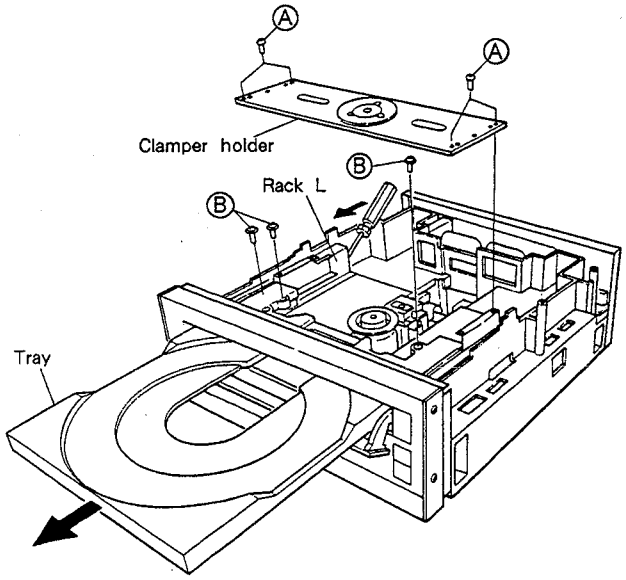


Fig. 7-4 Removing the tray and clamper holder

5. Removing the DACB, SRVD and SYPS assemblies

① Remove three screws Ⓐ from the DACB assembly.
② Remove eight screws Ⓑ from the SRVD assembly.
③ Remove four screws Ⓒ from the SYPS assembly and remove four screws Ⓓ of the heat sink from the rear.
Note : SYPS assembly is able to diagnosed that it is stood into the player.

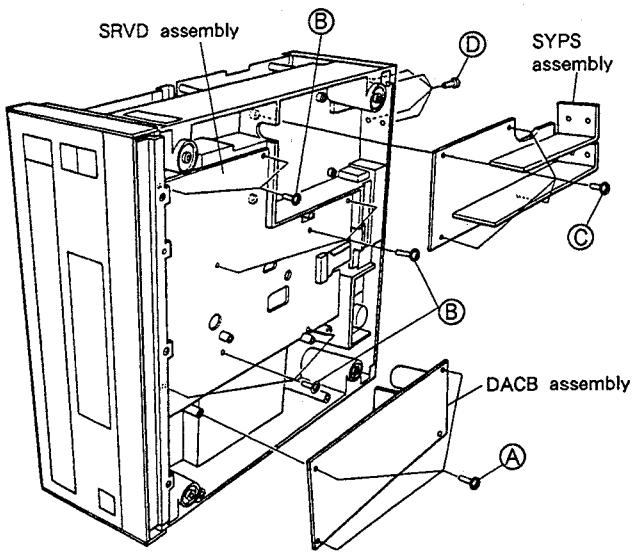


Fig. 7-5 Removing the DACB, SRVD and SYPS assemblies

– Notes on DACB assembly replacement –

When removing the DACB assembly (to repair the DACB assembly or to replace the mechanism chassis), be sure to short-circuit C11 and C12 (power smoothing capacitors) with a resistance of about 100ohms to discharge the capacitors.
If the DACB assembly is removed without doing this, the following trouble may occur.

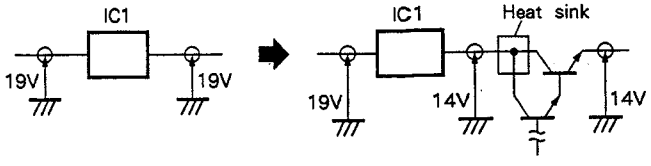
1. IC1 through IC4 (IC protectors) in the DACB assembly may be completely destroyed, or :
2. IC1 through IC4 (IC protectors) in the DACB assembly may be almost destroyed.

Case 1 can be easily recognized as the sound is cut off. For case 2 which may not show any immediate symptoms, check the following points.

Symptoms when the IC protectors have been almost destroyed (Case 2)

When the IC protectors are normal, the voltage at both ends is approx. 19V.

If the IC protectors are compro-mised, the electric potential becomes almost the same as that of the emission of the regulator transistor.



At the normal

At the compromise

6. Removing the mechanism assembly

① Disconnect the flexible cable which connecting between the SRVD assembly and the mechanism assembly from the SRVD assembly side (CN1).
② Remove four screws Ⓐ from the SRVD assembly.
③ Remove three screws Ⓑ from the mechanism assembly.
④ Disconnect two connectors CN6 and CN9 from the SRVD assembly.

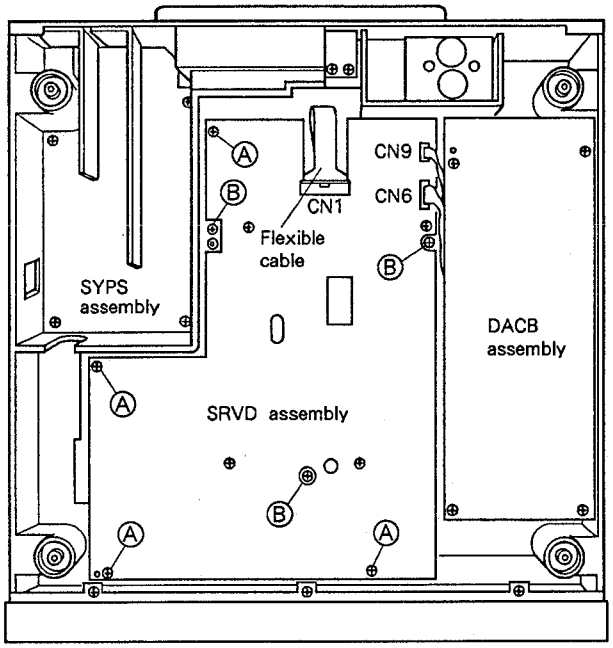


Fig. 7-6 Removing the mechanism assembly

7. Removing the pickup assembly

① Remove two screws from the pickup assembly.

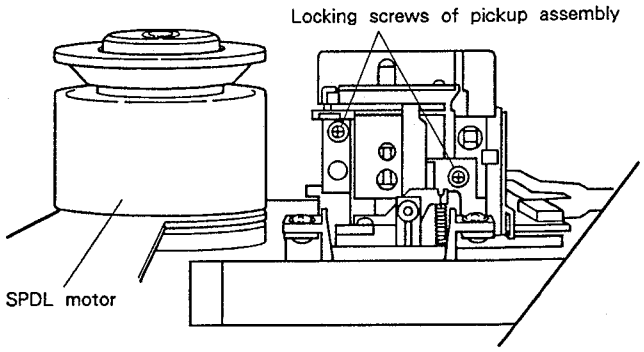


Fig. 7-7 Removing the pickup assembly

8. Removing the front panel assembly

① Remove three screws Ⓐ from the upper side of the front panel assembly and three screws Ⓑ from the lower side.

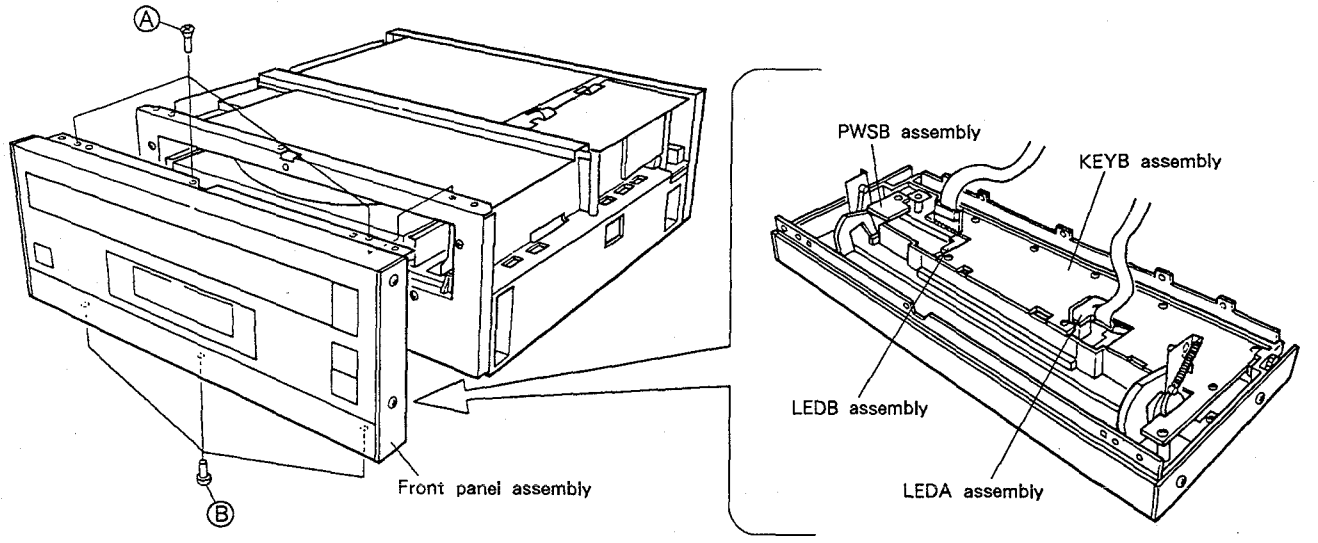


Fig. 7-8 Removing the front panel assembly

9. Removing the loading assembly

Note : The mechanism assembly should be removed first.
① Remove five screws Ⓐ from the upper side.
② Disconnect two connectors CN901 and CN903 from the LODV assembly.

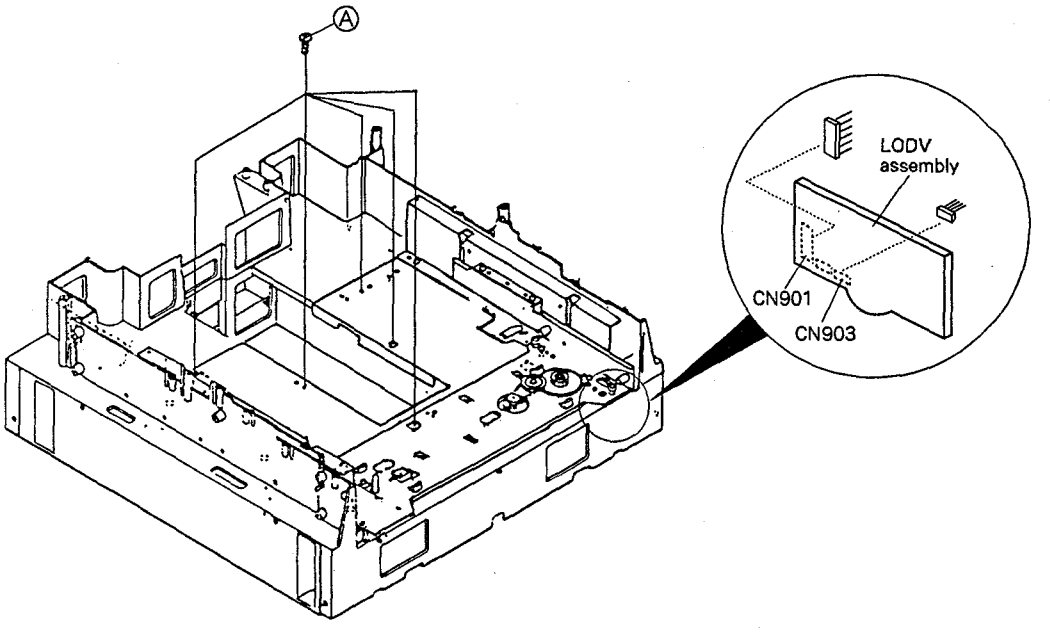


Fig. 7-9 Removing the loading assembly

8. TEST MODE

8.1 ENTRY OF THE TEST MODE

1. Turn the POWER switch ON.
2. Reject the carry by pressing the OPEN/CLOSE key.
3. Turn the POWER switch OFF.
4. Insert the carry in the player by pushing it by hand.
5. Close the front panel halfway by hand.
6. Turn the POWER switch ON.

8.2 RELEASE THE TEST MODE

Test mode can be released by the following two ways.

- [CX] + [9]
  (Press the remote control keys)
- Turn the POWER switch OFF.

8.3 FUNCTION OF THE TEST MODE

After the Test Mode is activated, the following functions will be engaged by pressing a combination of the CX key and a numeric key of the remote control.

[CX] + [0] : The FL display and LEDs light except DISPLAY OFF LED. (Toggle switch)
Because AC power of the FL (fluorescent) tube is turned on and off by the drive output of the DISPLAY OFF LED, the FL tube and DISPLAY OFF LED cannot be lit simultaneously.
The ROM version will be displayed on the screen of the monitor TV. (Toggle switch)

[CX] + [1] : Error rate measurement.
After the error rate is measured for 5 seconds, then the result will be displayed on the screen of the monitor TV. (complement and C1 and C2 error). Reject the key during measurement.

[CX] + [2] : Alternately opens and closes the tracking servo. (Toggle switch)

[CX] + [3] : Alternates the CX (noise reduction) circuit between CX default and default.
(toggle switch)

[CX] + [4] : Turns the tilt OFF forcibly.

[CX] + [5] : Turns the tilt ON.

[CX] + [6] : 3.0MHz oscillation ON and OFF (toggle switch) of the PD0011A : Output from PORT 3.

[CX] + [7] : Turns the LD (Laser Diode) ON and OFF during STOP.

[CX] + [8] : Not used.

[CX] + [9] : Release the Test Mode.

Other test mode functions

- In the Test Mode, lifting the clamper or ejecting the disc is impossible. However, if there is no disc on the tray, ejecting is possible.
- In the Test Mode, reject the Emergency port (57 of the expansion I/O) because of the power will be switched off.
- In the Test Mode, the initial search function can be released with the Clear key.
- In the Test Mode, search with the image remains on the screen will not be executed during test mode, search with gray back screen will be done instead.
- Open setup :
  The unit will be setup with tracking and tilt OPEN (off) when the unit is set to test mode during stop mode, then playback is started.
- Focus check :
  Setup of an LD can be executed without disc sensing when the PLAY key is pressed. During LD setup, the unit will wait a maximum of 9 seconds for the focus to be locked. Therefore, this function can be used to check the focus system in case disc sensing is not accomplished even with a disc inside.
- Focus and spindle lock checks are passed :
  The focus and spindle lock checks are not performed when the unit is set to test mode during playback mode.

① Focus lock check
····· Stop the spindle when the unit is defocused, and the unit waits until the focus is locked.

② Spindle lock check
····· Disc is ejected when the spindle unlock continued for 1 minute.

- Manual operation of the slider :
  The slider can be manually moved in the tracking open condition.
  Moving to the outer : SCAN FWD (▶▶) key of the unit
  Moving to the inner : SCAN REV (◀◀) key of the unit
  The slider is moved while pressing the SCAN key, and stopped it by depressing. Speed is able to set the four stages.
  Speed UP : INDEX SKIP FWD (→) key of the unit.
  Speed DOWN : INDEX SKIP REV (←) key of the unit.
- Picture quality adjustment and display OFF :
  In the Test Mode only, accept the remote control code as follows.

① Digital effect (5C) ··· Function is the same as the PICTURE key of the unit.
② File (0D) ····· Function is the same as the DISPLAY OFF key of the unit.

8.4 DISPLAY OF THE TEST MODE

In the Test Mode, the statuses of switches and other data are displayed on the screen of the monitor TV.

```
    0              1              2
    1234567890123456789012345678901234
 1  05    09. 12       i08  s01  □□
 2  05  02  09. 12      112  r05
 3  LD-on   F-1              TLT-on
 4  TRK-c1                F  c1  0104
 5  SPDL-1  run-noc           D-c1
 6
 7  IN (1)       OUT (0)
 8  TOP (0)
 9  MID (0)            SHP  TLMT  REL
10  BTM (1)             0    in    1
```

(TV monitor display in the frame)

[1st line]

Address information, internal mode and key code are displayed on the 1st line.

```
    0              1              2
    1234567890123456789012345678901234
    05    09. 12   i8  s01  112  □□
             ①          ②         ③
```

① Address information : Chapter and frame/time are displayed by the philips code.

② Internal mode : Display the each modes of the internal player.

- i8 IMODE : Major mode of internal

LOAD	0
OPEN	2
PARK	4
SETUP	6
PLAY	8
SEARCH	A (10)

- s01 SMODE : Minor mode in each IMODE.

③ Key code : Display the key code of the remote control and unit.

[2nd line]

Four indications are displayed on the 2nd line. Change the indication according to priority.

```
    0              1              2
    1234567890123456789012345678901234
 a  ERR   1234  5678
 b  LD-S2  VYW1467  9001130  M
 c  Chapter  07
 c  Frame  12345
 c  Time  03. 27
 d  01  12  03. 29
```

a. Error rate indication

b. ROM version indication (VYW1467, data, version)

c. Search point input mode (same as the normal search input mode.) and internal mode.

d. Subcode indication (only the disc with TOC)

- When the Test Mode is entered by the remote control, indicates "d".
- When the Test Mode is entered while opening the door at the POWER is ON, indicates "b" same as the CX + 0 key is pressed.
- Internal mode

  112 LKMODE : Tilt mechanism mode of the slider lock

  r05 RVMODE : Slider initialize mode

[3rd line]

```
    0              1              2
    1234567890123456789012345678901234
    LD-on   F-1              TLT-on
       off    u                  off
        ①     ②                  ③
```

Condition of the pickup section is displayed on the 3rd line.

① Laser diode indication
Display the laser diode on/off.

② Focus indication

Focus lock	l
Focus unlock	u

③ Tilt indication
Display the tilt servo on/off.

[4th line]

```
0              1              2
1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4
TRK-c1                    F  c1  0104
      op                  R  op
      ①                        ②
```

Condition of the tracking and slider sections are displayed on the 4th line.

① Tracking indication

Display the tracking servo open/close.

② Slider servo indication

- Display the direction of the slider.
  - F : FWD
  - R : REV
- Display the condition of the slider servo.
  - c1 : Loop close
  - op : Loop open
  - s1 : Speed 1 (very fast)
  - s2 : Speed 2 ↓
  - s3 : Speed 3 ↓
  - s4 : Speed 4 (very slow)
- Slit address position of the slider.

  Display the slit address with hexadecimal number system.
  - 0000→0220
  - Inner→Outer

[5th line]

```
0              1              2
1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4
SPDL-1  run-noc                  D-c1
      u  off  ac1                  op
                brk
        ①                        ②
```

Condition of the spindle and door switch are displayed on the 5th line.

① Spindle indication

Display the lock/unlock, run/off, accelerate/brake, and etc. of the spindle.

- 1 : Spindle lock
- u : Spindle unlock
- s : Spindle stop
- run : Spindle run
- off : Spindle free run
- acl : Accelerate
- brk : Brake
- noc : No control (control by TBC)

② Door switch indication

Display the condition of the door switch.

- c1 : Door close
- op : Door open

[7th thru 10th lines]

Loading section is displayed on the 7th thru 10th lines.

Display the horizontal movement of the carry on the 7th line.

- (0) : SW OFF
- (1) : SW ON

Display the arrow during moving the carry.

- Loading : ←
- Unloading : →

Display the vertical movement of the carry on the left side of the 8th thru 10th lines.

- (0) : SW OFF
- (1) : SW ON

Display the arrow during moving the carry.

- Carry UP : ↑
- Carry DOWN : ↓

Display the tilt and slider lock mechanism on the right side of the 9th and 10th lines.

- 0 : SW OFF
- 1 : SW ON
- in : within the limits of the tilt limit
- over : beyond the limits of the tilt limit

Display the arrow during operating the mechanism.

- Release : ↑
- Lock : ↓

8.5 ENTRY OF THE MANUAL MODE

In addition to test mode, manual mode to individually move the motors is availabale.

8.6 RELEASE THE MANUAL MODE

Manual mode can be released by the following two ways.

1. [CX] + [9]
2. Turn the POWER switch OFF.

8.7 FUNCTION OF THE MANUAL MODE

After the Manual Mode is activated, the following functions will be engaged by this unit key.

① Horizontal movement of the carry
- Loading : DISPLAY OFF key of the unit
- Unloading : PICTURE key of the unit

② Vertical movement of the carry
- Carry UP : OPEN · CLOSE key of the unit
- Carry DOWN : PLAY/STILL key of the unit

③ Operation of the tilt and slider lock mechanism
- Release : CHAPTER SKIP FWD (▶▶|) key of the unit
- Lock : CHAPTER SKIP REV (|◀◀) key of the unit

④ Stop

When the STOP key is pressed while motors ①, ② and ③ are operating, the motors stop.

* The motors also stop when the SW condition of either of the motors changes during operation.

⑤ Manual operation of the slider

Moving to the outer: SCAN FWD (▶▶) key of the unit
Moving to the inner: SCAN REV (◀◀) key of the unit
The slider is moved while pressing the SCAN key, and stopped it by depressing.
Speed is able to set the four stages.
Speed UP : INDEX SKIP FWD (⌁) key of the unit.
Speed DOWN: INDEX SKIP REV (⌁) key of the unit.

8.8 DISPLAY OF THE MANUAL MODE

In the Manual Mode, the statuses of switches and other data are displayed on the screen of the monitor TV.

```
    0              1              2
    1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4
 1 MANUAL MODE                              □□
 2 LD-S2 VYW1467 900113a M
 3 LD-off F-u                          TLT-off
 4 TRK-op                          F op 0104
 5 SPDL-u off-noc                      D-op
 6
 7 IN (1)        OUT (0)
 8 TOP (0)
 9 MID (0)                SHP TLMT REL
10 BTM (1)                 0   in   1
```

(TV monitor display in the frame)

Display is the same as the Test Mode except displaying the "MANUAL MODE" on the 1st line.

9. ADJUSTMENTS

9.1 JIGS AND INSTRUMENTS REQUIRED FOR ADJUSTMENT

- Small ⊖ screwdriver (about 7 cm long)
- Small Philips head screwdriver (at least 15 cm long)
- Low-pass filter (100k ohms + 1 μF/BP)
- Dual-trace oscilloscope (with delay)
- AF generator
- Frequency counter
- Test disc (GGV1002)
- LDD disc (buy locally)
- Shorting clip
- TV Monitor
- Resistors (100k ohms and 330k ohms)
- Capacitor (0.01 μF)
- Post for the mechanism adjustment (GGF1048)
- Disc clamper (VXX1354)
- Eccentric screwdriver (GGV-134)
- Hexagonal wrench (2 mm)

9.2 PREPARATIONS FOR ADJUSTMENT AND PRECAUTIONS

9.2.1 Setting of the player when performing the mechanism adjustment

Install the post for the mechanism assembly (hereinafter referred to as "POST") (GGF1048) after the mechanism assembly is took out from the player. When the disc is playbacked, install the disc clamper (VXX1354). Check the parts on the SRVD assembly by placing a mirror or equivalent between the feet of POST.

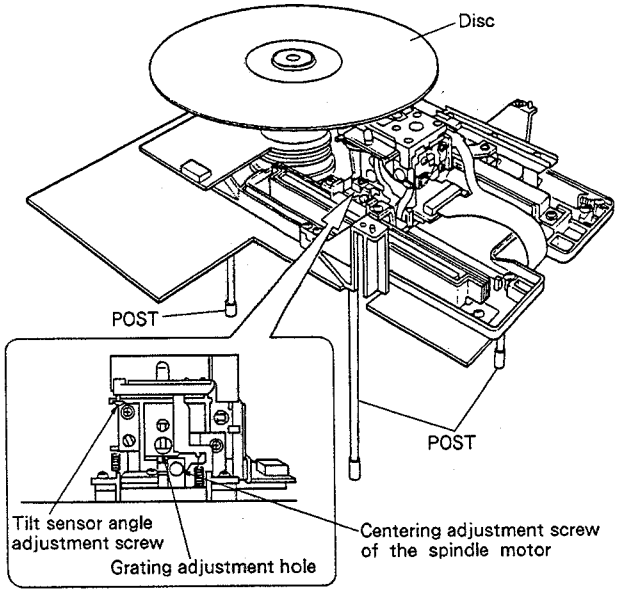


Fig. 9-1

9.2.2 Procedure of the mechanism adjustments

1. FOCS offset adjustment
2. Linear offset adjustment
3. Coarse grating and TRKG (tracking) balance adjustment
4. TRKG direction inclination adjustment of the pickup assembly (*1)
5. TAN (tangential) direction inclination adjustment of the pickup assembly (*1)
6. Height adjustment of the pickup assembly
7. Tilt base horizontal adjustment
8. Fine TRKG direction inclination adjustment of the pickup adjustment
9. Fine TAN direction inclination adjustment of the pickup assembly
10. FOCS (focus) balance adjustment
11. SPDL (spindle) motor centering check (*2)
12. SPDL motor centering adjustment (*2)
13. Fine grating and TRKG balance adjustment
14. Tilt sensor inclination adjustment
15. RF level adjustment
16. Silent FOCS adjustment
17. FOCS gain adjustment
18. TRKG servo loop gain adjustment

*1 : Adjustment items 4 and 5 are not performed when the pickup is replaced, its should be performed when the pickup base is disassembled.

*2 : Adjustment items 11 and 12 are checked and adjusted the position of the pickup against the centering line of the spindle motor.

9.2.3 About the shipping lock of the pickup assembly

Shipping lock/release of the pickup assembly is switched by switching the Pickup lock and release switches of the mechanism assembly. Shipping is automatically locked when the POWER switch is turned OFF.

Note that the pickup assembly is not fixed if the main unit is unplugged before turning off the POWER switch. If the unit is not level with the pickup assembly unfixed, the pickup may be damaged.

In addition, be sure to set the unit in the shipping lock state when removing the mechanism assembly.

9.2.4 How to lock/release the shipping of the pickup assembly

When the shipping is locked and released forcibly, connect a battery to the terminal of the tilt motor as shown in Fig. 9-2 and change the two switches by rotating the tilt motor. At this time, CN9 should be disconnected.

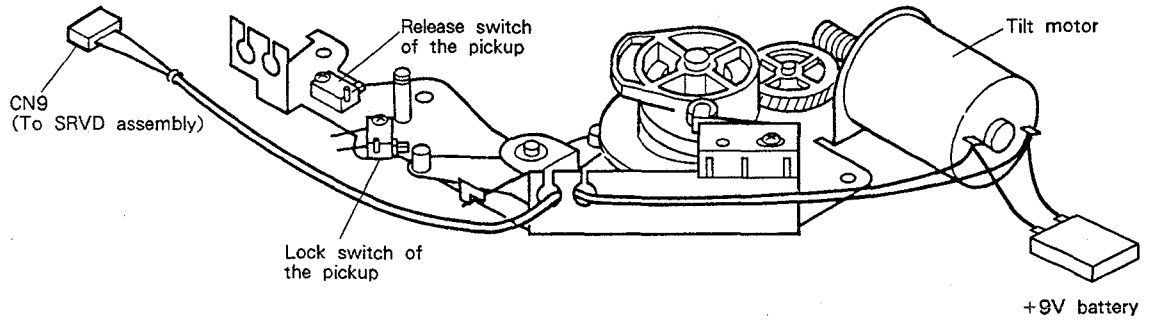


Fig. 9-2

9.2.5 Test disc for the adjustment should be used the GGV1002.

9.2.6 The oscilloscope should be used with a 10 : 1 probe.

9.2.7 When the disc is playbacked at the test mode, start the playback with the tracking servo is opened.

9.2.8 Do not touch the slider shaft with bare hands. When touching it, be sure to wear clean gloves.

Note : Should it have been touched by bare hands, swab it with absolute alcohol.

9.2.9 About the abbreviation in the adjustment

FOCS → Focus
TRKG → Tracking
SPDL → Spindle
SLDR → Slider
TAN → Tangential
POST → Post for the mechanism assembly

9.3 MECHANISM ADJUSTMENT

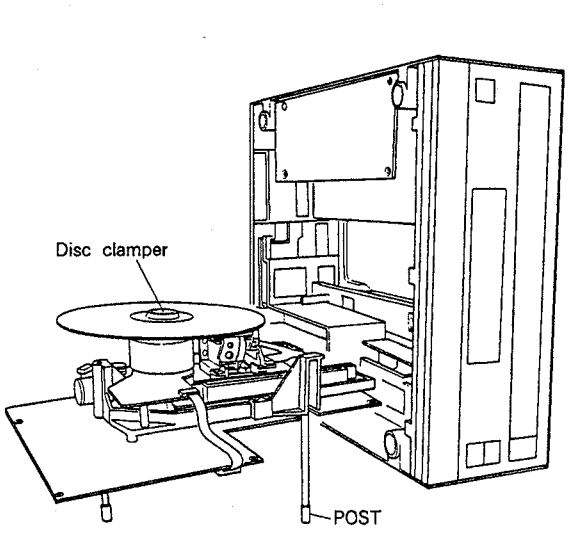
1. FOCS Offset Adjustment

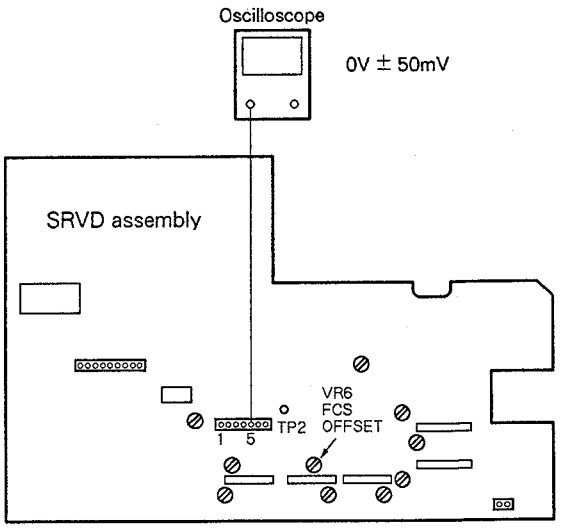
● Purpose : To set the offset voltage of the focus servo loop to 0V.

● When not properly adjusted : Picture distored.

● Measuring instruments and jigs	● Oscilloscope ● POST
● Measuring point	● SRVD assembly TP2-5 (FOCS ERR)
● Test disc and player mode	● Turn POWER switch ON ● Standby condition
● Position to be adjusted	● SRVD assembly VR6

Connection diagram





Adjustment procedure

1. Turn the POWER switch ON to the standby condition.
2. Adjust VR6 in the SRVD assembly so that the DC voltage of TP2-5 becomes 0V ± 50mV.
   (Connect GND of the oscilloscope to TP2-1)

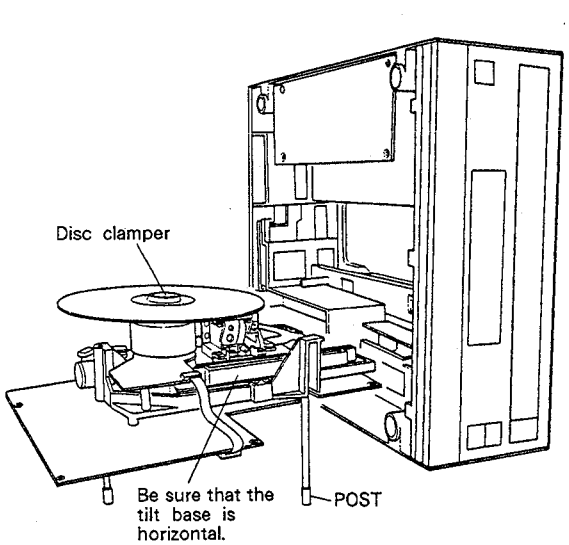
2. Linear Offset Adjustment

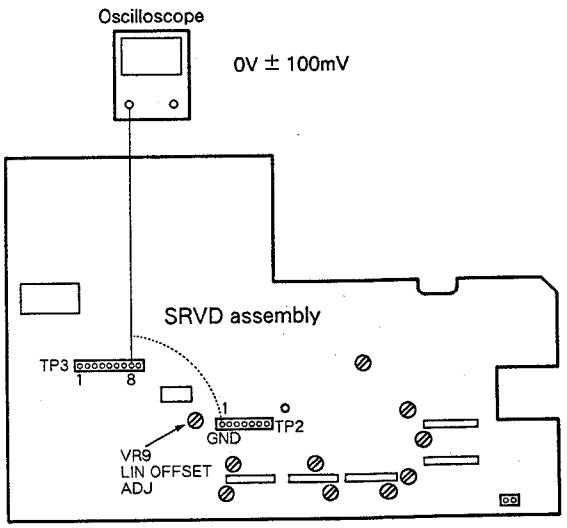
● Purpose : To set the offset voltage of the linear servo loop to 0V.

● When not properly adjusted : When the POWER switch is turned ON, the pickup assembly will be moved to the inner or the outer tracks.

● Measuring instruments and jigs	● Oscilloscope ● POST
● Measuring point	● SRVD assembly TP3-8 (Linear drive)
● Test disc and player mode	● Turn the POWER switch ON ● Standby condition
● Position to be adjusted	● SRVD assembly VR9

Connection diagram

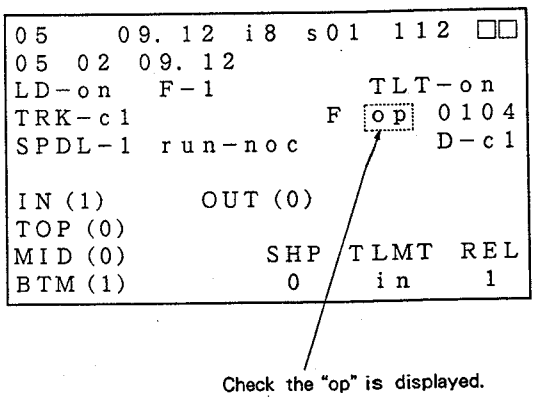




Adjustment procedure

1. Check that the tilt base is set horizontally.
2. Set the player to the Test Mode. (See page 96.)
3. Check that on the test mode display "op" is displayed next to "F" or "R" on the forth row from the top of the screen.
4. Adjust VR9 in the SRVD assembly so that the voltage of TP3-8 (Linear drive) becomes 0V ± 100mV.

Note : If the TV sync signal is carried on the linear drive waveform and disturbs the adjustment, turn off power of the adjacent TV set.



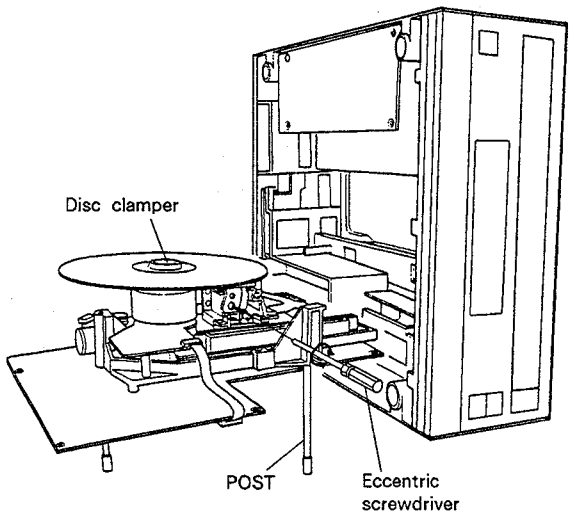
3. Coarse Grating and TRKG Balance Adjustment

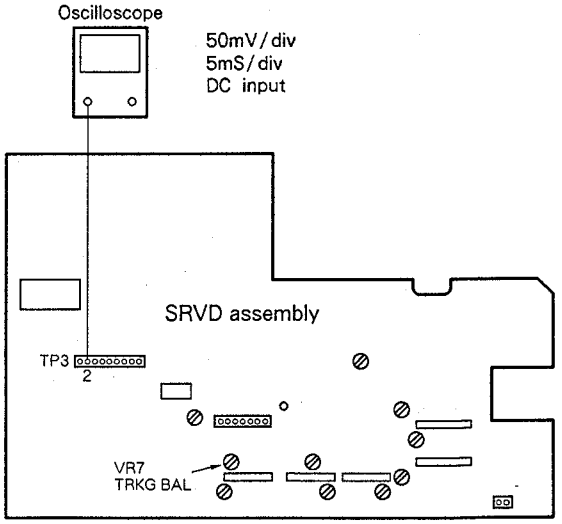
● Purpose : To adjust the grating for the disc playback will be possible.

● When not properly adjusted : Disc playback will be impossible. Picture distored.

● Measuring instruments and jigs	● Oscilloscope ● Test disc (GGV1002) ● POST ● Disc clamper ● Eccentric screwdriver
● Measuring point	● SRVD assembly TP3-2 (TRKG ERR)
● Test disc and player mode	● Around #15,000 ● Test mode : TRKG servo open (CX 2)
● Position to be adjusted	● Grating ● SRVD assembly VR7 (TRKG error balance)

Connection diagram





Adjustment procedure

1. Set the GND of the oscilloscope to the center.
2. Set the player to the Test Mode.
3. Set the test disc and press the PLAY key. Move the pickup to around frame #15,000 using SCAN key of the remote control. (TRKG servo is opened.)
4. Connect TP3-2 in the SRVD assembly to the CH1 of the oscilloscope and observe the TRKG error waveform. Adjust the grating by the eccentric screwdriver to the position (ON-track position) where the waveform amplitude becomes minimum with a smooth envelope. (Photo 1)
5. Slowly turn the eccentric screwdriver clockwise and stop turning at the point where the amplitude of the TRKG error waveform becomes maximum for the first time.
6. Adjust VR7 in the SRVD assembly so that the amplitude "a" and "b" of the TRKG error waveform become equal (DC0V). (Photo 2)
7. Close the TRKG servo and check that the picture on the TV monitor appears normal.

Note: If the pickup moves with the TRKG servo opend, disturbing the adjustment, perform "2. Linear Offset Adjustment" with the TRKG servo open and after all the mechanical adjustments are completed, repeat "2. Linear Offset Adjustment," this time in the POWER ON state only. (See page 103.)

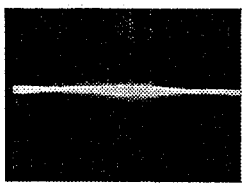


Photo 1
On-track position

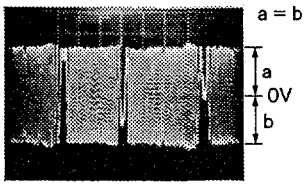


Photo 2
Maximum amplitude

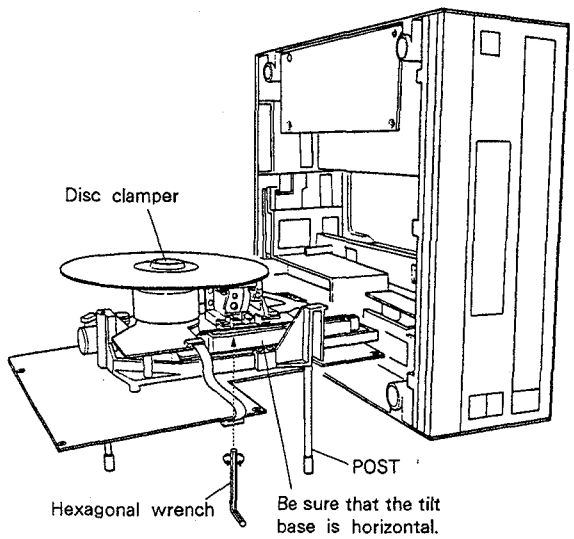
4. TRKG Direction Inclination Adjustment of the Pickup Assembly

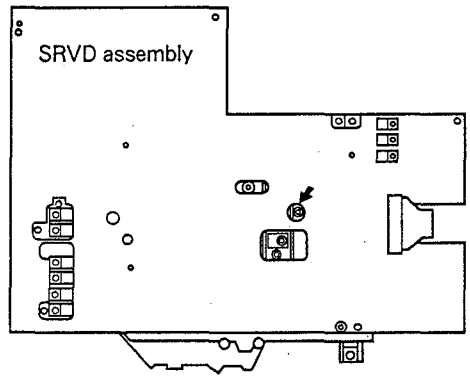
Mechanism Adjustment

● Purpose : To adjust the inclination of the pickup assembly in the center direction of the disc to the horizontal position.
● When not properly adjusted : Crosstalk will be generated.

● Measuring instruments and jigs	● Test disc (GGV1002) ● Hexagonal wrench ● TV monitor ● POST ● Disc clamper
● Measuring point	
● Test disc and player mode	● #115 still ● Test mode : Tilt servo OFF (CX 4), TRKG servo close (CX 2)
● Position to be adjusted	● TRKG direction inclination adjustment screw of the pickup assembly

Connection diagram

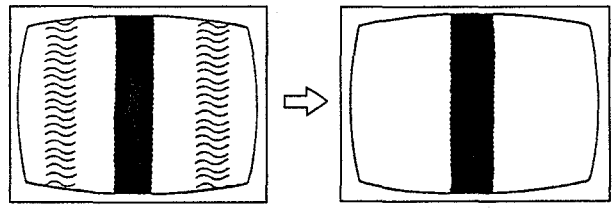




TRKG direction inclination adjustment screw of the pickup assembly.

Adjustment procedure

1. Check that the tilt base is set horizontally.
2. Set the player to the Test Mode.
3. Set the tilt servo to OFF forcibly.
4. Play the test disc (GGV1002) and search frame #115.
5. Adjust the TRKG direction inclination adjustment screw of the pickup assembly so that the crosstalk on the left and right sides on the TV screen becomes minimum.



Crosstalk on the screen — Crosstalk becomes minimum

Adjust so that the crosstalk on the screen becomes minimum.

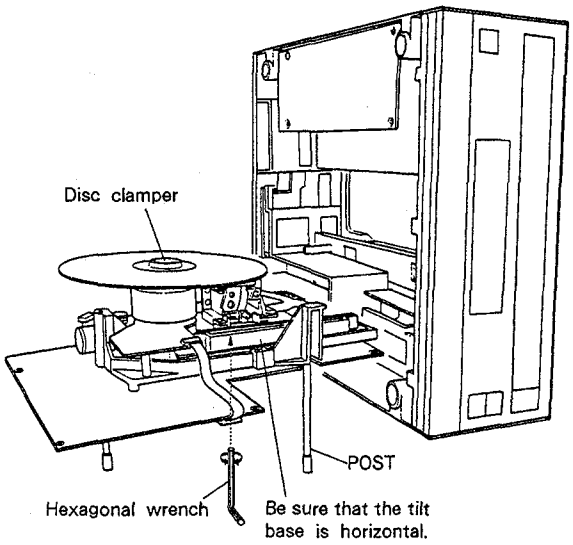
5. TAN Direction Inclination Adjustment of the Pickup Assembly

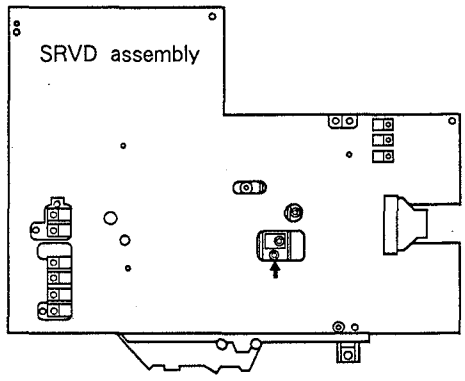
Mechanism Adjustment

● Purpose : To adjust the inclination of the pickup assembly in the tangential direction of the disc tracks to the horizontal position.
● When not properly adjusted : Crosstalk will be generated.

● Measuring instruments and jigs	● Test disc (GGV1002) ● TV monitor ● Hexagonal wrench (2mm) ● POST ● Disc clamper
● Measuring point	
● Test disc and player mode	● #115 still ● Test mode : Tilt servo OFF ([CX][4]), TRKG servo close ([CX][2])
● Position to be adjusted	● TAN direction inclination adjustment screw of the pickup assembly.

Connection diagram

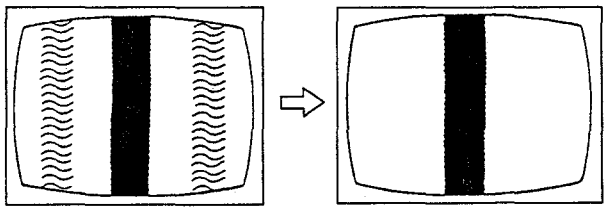




TAN direction inclination adjustment screw of the pickup assembly

Adjustment procedure

1. Check that the tilt base is set horizontally.
2. Set the player to the Test Mode.
3. Set the tilt servo to OFF forcibly.
4. Play the test disc (GGV1002) and search frame #115.
5. Adjust the TAN direction inclination adjustment screw of the pickup assembly so that the crosstalk on the left and right sides on the TV screen becomes minimum.



Crosstalk on the screen — Crosstalk becomes minimum

Adjust so that the crosstalk on the screen becomes minimum.

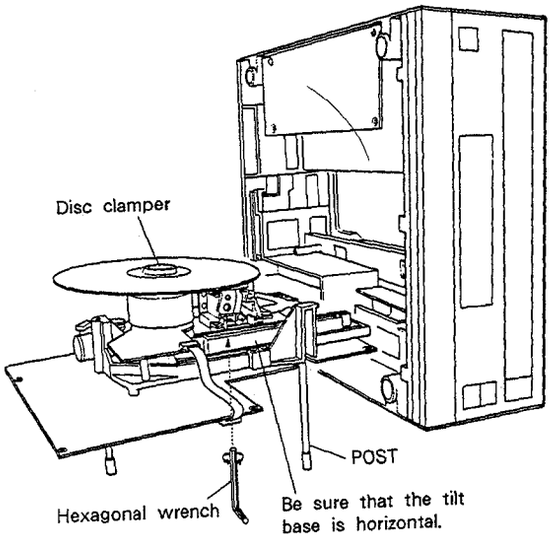
6. Height Adjustment of the Pickup Adjustment

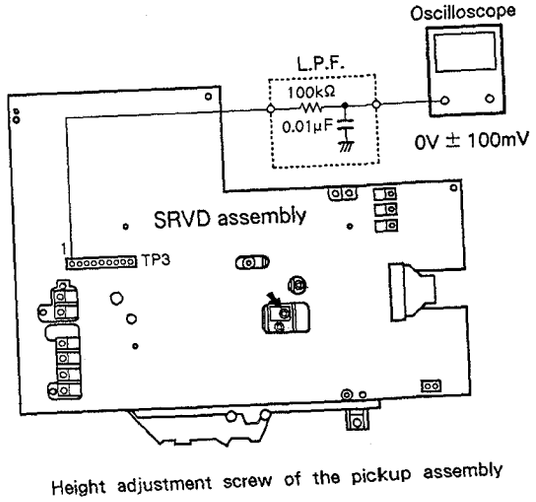
● Purpose : To adjust the height of the pickup assembly so that the laser beam is accurately focused on the signal surface (bits) of the disc

● When not properly adjusted : Disc playback will be impossible. Crosstalk will be generated.

● Measuring instruments and jigs ● Measuring point ● Test disc and player mode ● Position to be adjusted	● Test disc (GGV1002) ● Hexagonal wrench ● POST ● Disc clamper ● L. P. F. ● SRVD assembly TP3-1 (FOCS DRV) ● Oscilloscope ● #10,000 (Tilt fulcrum) still ● Test mode : Tilt servo OFF (CX 4), TRKG servo close (CX 2) ● Height adjustment screw of the pickup assembly.

Connection diagram





Adjustment procedure

1. Set the player to the Test Mode.
2. Set the tilt servo to OFF forcibly.
3. Connect TP3-1 (FOCS DRV) in the SRVD assembly to the oscilloscope via the L.P.F.
4. Close the TRKG servo and play the test disc (GGV1002), then search frame #10,000 (STILL mode).
5. Adjust the height adjustment screw of the pickup assembly so that the voltage of TP3-1 in the SRVD assembly becomes 0V ± 100mV.

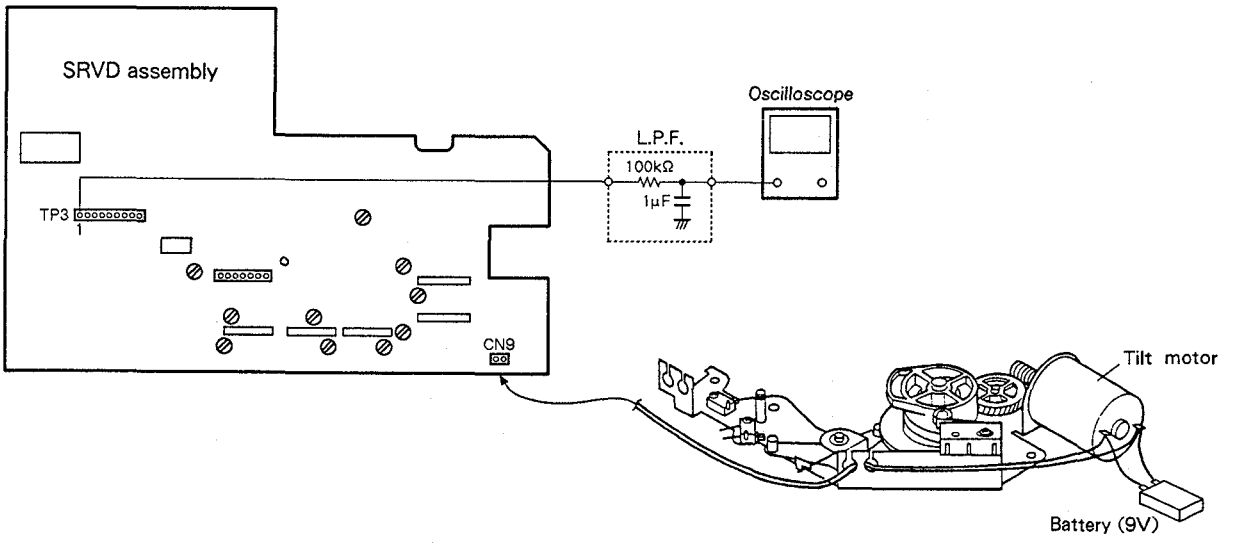
7. Tilt Base Horizontal Adjustment

Mechanism Adjustment

● Purpose : In disc playback, make the tilt base horizontal so that the FOCS servo can sufficiently operate both at the inner track and outer track.
● When not properly adjusted : Picture distored at the inner or outer of the disc.

● Measuring instruments and jigs	● Oscilloscope ● Test disc (GGV1002) ● POST ● Disc clamper ● L. P. F. ● Battery (9V) and lead wire
● Measuring point	● SRVD assembly TP3-1 (FOCS DRV)
● Test disc and player mode	● Still at the inner and outer of the disc. ● Test mode : Tilt servo OFF (CX 4), TRKG servo close (CX 2)
● Position to be adjusted	● Tilt motor

Connection diagram



Adjustment procedure

1. Set the player to the Test Mode.
2. Set the tilt servo to OFF forcibly.
3. Connect TP3-1 (FOCS DRV) in the SRVD assembly to the oscilloscope via the L.P.F.
4. Play the test disc and search frame #10,000 (STILL mode) and measure the FOCS drive voltage.
5. Next, search frame #100 (STILL mode) and measure the FOCS drive voltage.
6. Check that the FOCS drive voltage difference between step 4 and 5 is within ± 90mV.
7. If it is not within ± 90mV, connect a battery to the tilt motor and turn the motor until the FOCS drive voltage becomes within ± 90mV.(At this time, CN9 should be disconnected.)

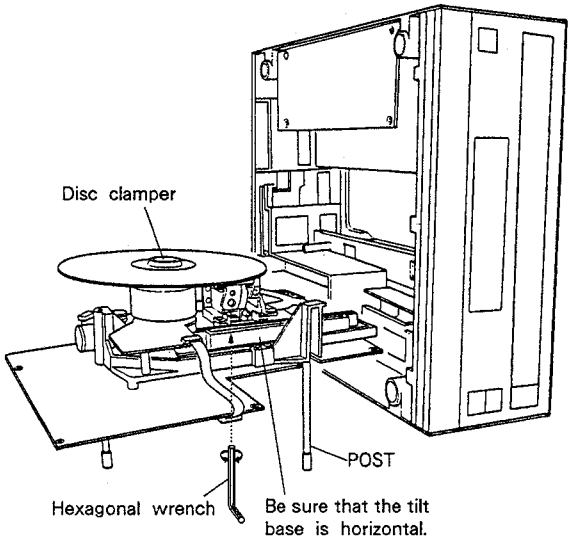
8. Fine TRKG Direction Inclination Adjustment of the Pickup Adjustment

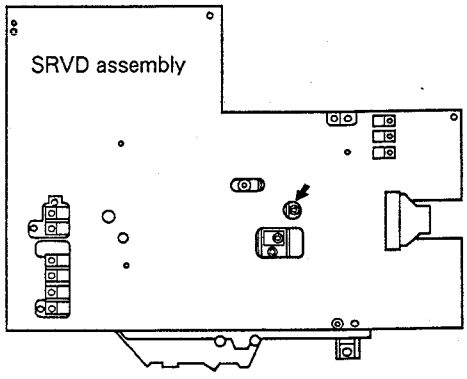
Mechanism Adjustment

● Purpose : To adjust the inclination of the pickup assembly in the TRKG direction of the disc to the horizontal position.
● When not properly adjusted : Crosstalk will be generated.

● Measuring instruments and jigs	● TV monitor ● Test disc (GGV1002) ● POST ● Disc clamper ● Hexagonal wrench (2mm)
● Measuring point	
● Test disc and player mode	● #115 still ● Test mode : tilt servo OFF (CX 4), TRKG servo close (CX 2)
● Position to be adjusted	● TRKG direction inclination adjustment screw of the pickup assembly.

Connection diagram

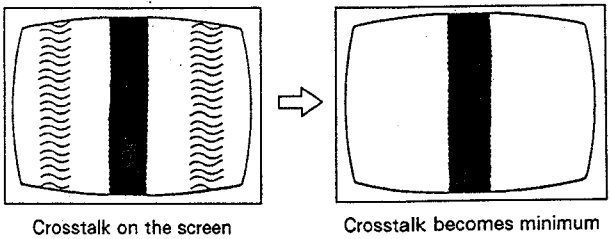




TRKG direction inclination adjustment screw of the pickup assembly.

Adjustment procedure

1. Check that the tilt base is set horizontally.
2. Set the player to the Test Mode.
3. Set the tilt servo to OFF forcibly.
4. Play the test disc (GGV1002) and search frame #115.
5. Adjust the TRKG direction inclination adjustment screw of the pickup assembly so that the crosstalk on the left and right sides on the TV screen becomes minimum.



Crosstalk on the screen — Crosstalk becomes minimum

Adjust so that the crosstalk on the screen becomes minimum.

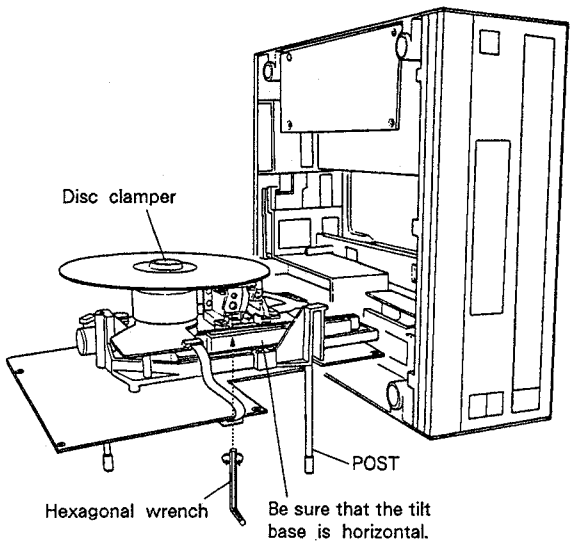
9. Fine TAN Direction Inclination Adjustment of the Pickup Assembly

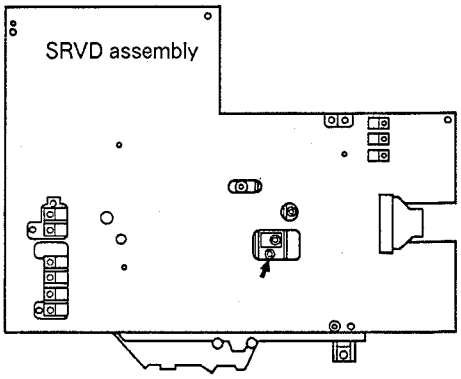
Mechanism Adjustment

● Purpose : To adjust the inclination of the pickup assembly in the tangential direction of the disc tracks to the horizontal position.
● When not properly adjusted : Crosstalk will be generated.

● Measuring instruments and jigs	● Test disc (GGV1002) ● TV monitor ● Hexagonal wrench (2mm) ● POST ● Disc clamper
● Measuring point	
● Test disc and player mode	● #115 still ● Test mode : Tilt servo OFF ([CX][4]), TRKG servo close ([CX][2])
● Position to be adjusted	● TAN direction inclination adjustment screw of the pickup assembly.

Connection diagram

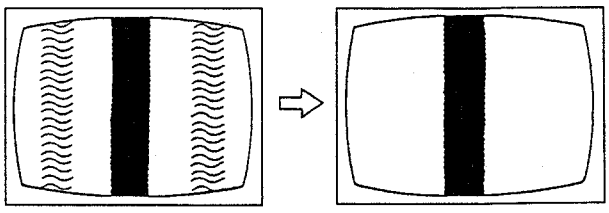




TAN direction inclination adjustment screw of the pickup assembly.

Adjustment procedure

1. Check that the tilt base is set horizontally.
2. Set the player to the Test Mode.
3. Set the tilt servo to OFF forcibly.
4. Play the test disc (GGV1002) and search frame #115.
5. Adjust the TAN direction inclination adjustment screw of the pickup assembly so that the crosstalk on the left and right sides on the TV screen becomes minimum.



Crosstalk on the screen — Crosstalk becomes minimum

Adjust so that the crosstalk on the screen becomes minimum.

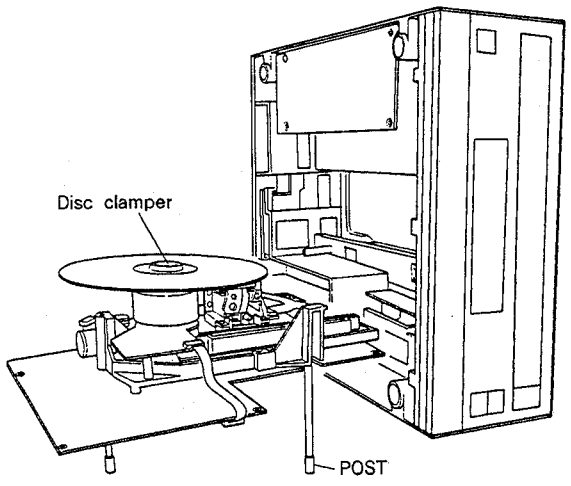
10. FOCS Balance Adjustment

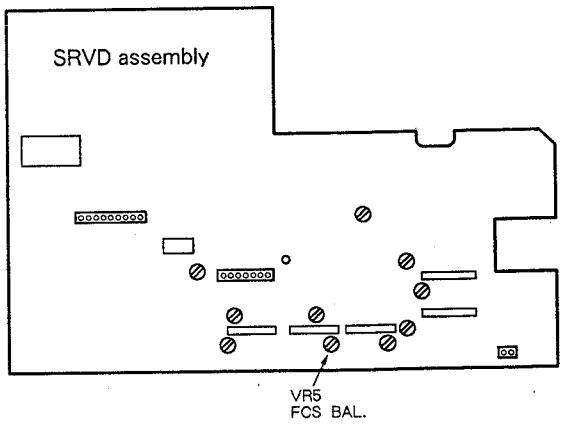
● Purpose : To adjust the balance of the FOCS servo electrically.

● When not properly adjusted : Crosstalk.

● Measuring instruments and jigs	● TV monitor ● Test disc (GGV1002) ● POST ● Disc clamper
● Measuring point	
● Test disc and player mode	● #115 still ● Test mode : Tilt servo OFF (CX 4), TRKG servo close (CX 2)
● Position to be adjusted	● SRVD assembly VR5

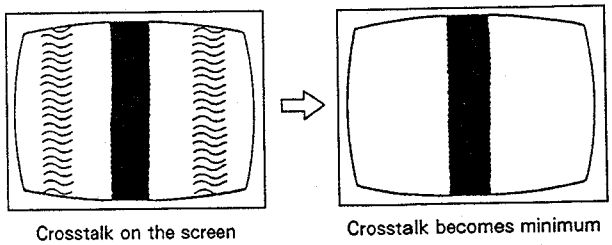
Connection diagram





Adjustment procedure

1. Set the player to the Test Mode.
2. Set the tilt servo to OFF forcibly.
3. Close the TRKG servo and play the test disc, then search frame #115.
4. Adjust VR5 so that the crosstalk on the left and right sides on the TV screen becomes minimum.



Crosstalk on the screen — Crosstalk becomes minimum

Adjust so that the crosstalk on the screen becomes minimum.

11. SPDL Motor Centering Check

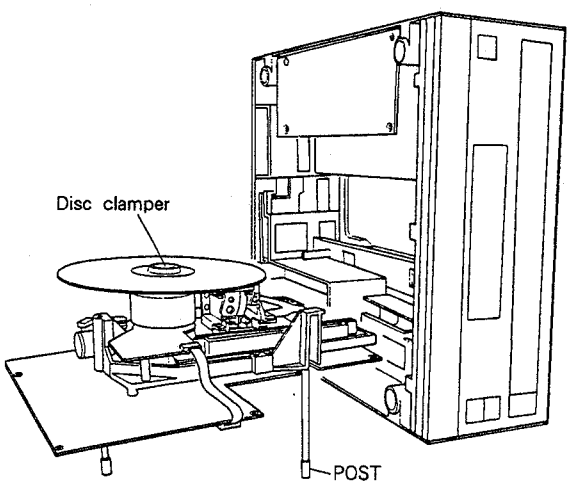
Mechanism Adjustment

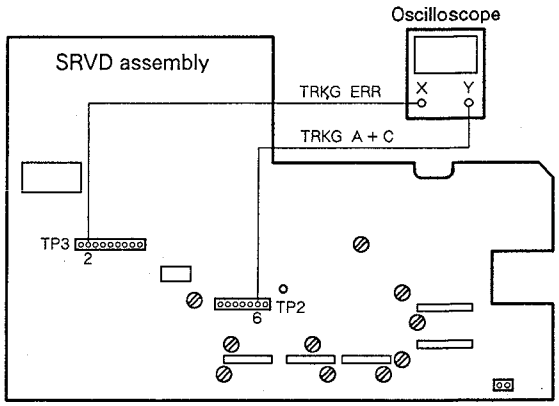
● Purpose : To check that the center of the spindle motor is on the orbit of the laser beam.

● When not properly adjusted : Track skips, or searching takes too long.

● Measuring instruments and jigs	● Oscilloscope ● Test disc (GGV1002) ● POST ● Disc clamper
● Measuring point	● SRVD assembly CH1 : TP3-2 (TRKG ERR), CH2 : TP2-6 (TRKG A + C)
● Test disc and player mode	● Test mode : TRKG servo open (CX 2), Tilt servo OFF (CX 4)
● Position to be adjusted	

Connection diagram





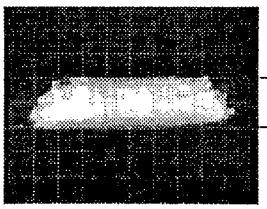


Photo 3 Lissajous figure of the inner track of the disc

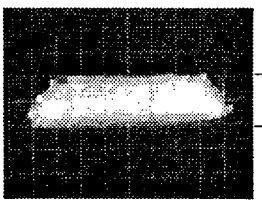


Photo 4 Lissajous figure of the outer track of the disc

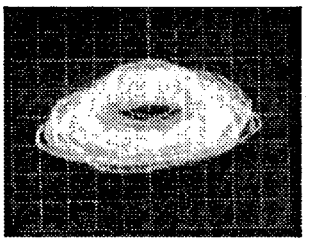


Photo 5 Lissajous figure when not properly adjusted

Checking Procedure

Note : In this item, check that the position of the pickup assembly to the center of the spindle motor.

1. Set the player to the Test Mode and play the test disc. (Rising up with TRKG servo is opened.)
2. Connect TP3-2 (TRKG ERR) in the SRVD assembly to the CH1 (X input) of the oscilloscope and TP2-6 (TRKG A + C) to the CH2 (Y input).
3. Set the oscilloscope to the X-Y mode and observe the Lissajous figures of the TRKG error signal and TRKG (A + C) signal.
4. Check that the amplitude of the Lissajous figures at the inner and outer tracks of the disc are same.

Note : If the amplitude of the Lissajous figure is different for the inner and outer tracks, perform "12. SPDL motor centering adjustment".

12. SPDL Motor Centering Adjustment

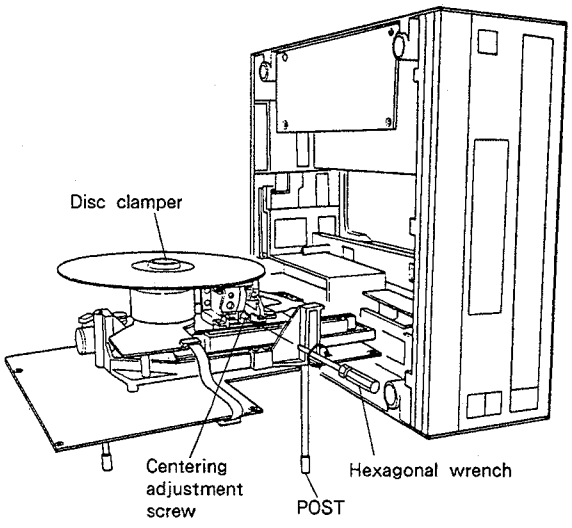
Mechanism Adjustment

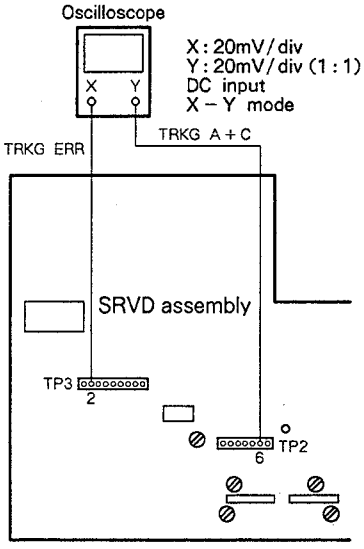
● Purpose : To adjust so that the center of the spindle motor is on the orbit of the laser beam.

● When not properly adjusted : Track skips, or searching takes too long.

● Measuring instruments and jigs	● Oscilloscope ● Test disc (GGV1002) ● Hexagonal wrench (2mm) ● POST ● Disc clamper
● Measuring point	● SRVD assembly CH1 : TP3-2 (TRKG ERR), CH2 : TP2-6 (TRKG A + C)
● Test disc and player mode	● #20,000 still ● Test mode : TRKG servo open ([CX][2]), Tilt servo OFF ([CX][4])
● Position to be adjusted	● Centering adjustment screw in the mechanism assembly.

Connection diagram





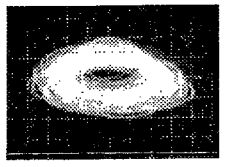


Photo 6

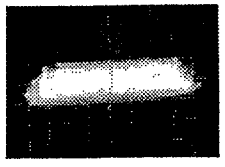


Photo 7

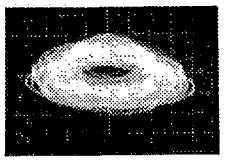


Photo 8

Adjustment procedure

Note 1 : Adjust that the position of the pickup assembly to the center of the spindle motor.

Note 2 : This adjustment is performed only when the "11. SPDL motor centering check is insufficiency.

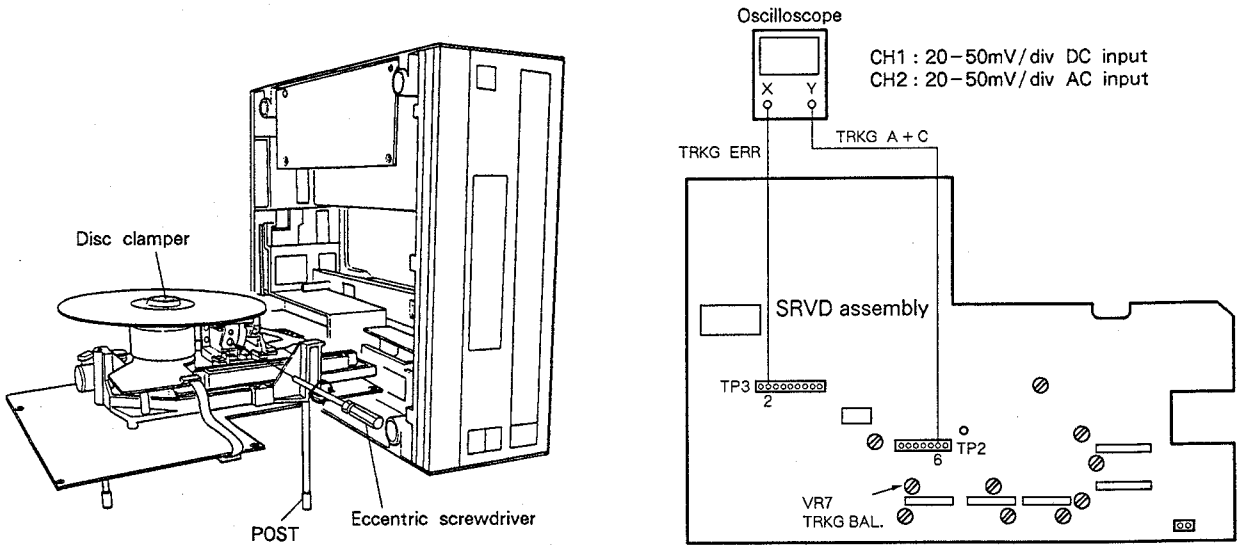
1. Connect TP3-2 in the SRVD assembly to the CH1 (X input) of the oscilloscope and TP2-6 to the CH2 (Y input).
2. Set the player to the Test Mode and press the [CX] and [4] keys (tilt servo OFF) of the remote control, then play the test disc.
3. Search around frame #20,000 (STILL mode) and observe the Lissajous figures of the TRKG error signal and TRKG (A + C) signal.
4. Fine-adjust the grating so that the Y-axis amplitude of the Lissajous figure is minimized.
5. Move the pickup assembly to the inner track of the disc by pressing the SCAN and REV keys.
6. Observe the Lissajous figure and write down the Y-axis amplitude.
7. Move the pickup assembly to the outer track again. Turn the centering adjustment screw clockwise using the hexagonal wrench, and turn slowly so that the Y-axis amplitude of the Lissajous figure is reduced. After the Y-axis amplitude of the Lissajous figure is minimized, turn the adjustment screw further until the amplitude becomes the same shape as that observed in procedure 6.
8. Move the pickup assembly to the outer track of the disc by pressing the SCAN and FWD keys.
9. Observe the Lissajous figure to check that the Y-axis amplitude is minimum. If the Y-axis amplitude of the Lissajous figure is larger than specified, repeat the adjustment procedures from steps 3 to 8.

13. Fine Grating and TRKG Balance Adjustment

● Purpose : To fine adjust the grating so that the two tracking beams for the TRKG servo are projected in the optimum positions on the tracks being played.
● When not properly adjusted : Track skips.

● Measuring instruments and jigs	● Oscilloscope ● Eccentric screwdriver ● POST ● Disc clamper
● Measuring point	● SRVD assembly CH1 : TP3-2 (TRKG ERR), CH2 : TP2-6 (TRKG A + C)
● Test disc and player mode	● Test mode : TRKG servo open (CX 2) ● Around #15,000 still
● Position to be adjusted	● Grating adjustment hole of the pickup assembly ● SRVD assembly VR7

Connection diagram

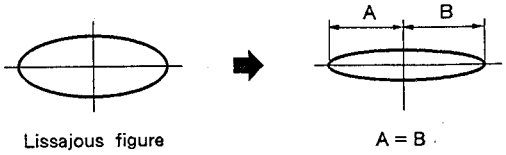


Adjustment procedure

1. Set the player to the Test Mode.
2. Play the test disc and search around frame #15,000 by SCAN key. (TRKG servo open)
3. Connect TP3-2 in the SRVD assembly to the CH1 (X input) of the oscilloscope and TP2-6 to the CH2 (Y input).
4. Observe the Lissajous figure and fine-adjust the Y-axis amplitude is minimized.
5. Adjust VR7 in the SRVD assembly so that the "A" and "B" of the Lissajous figure become equal (A = B).
6. Close the TRKG servo by pressing the CX and 2 keys of the remote control, and check that the picture (image) on the TV screen is normal.

Note 1 : The grating has been adjusted at the factory for the track pitch of 1.35μm of normal discs. As the test disc GGV1002 (track pitch : 1.52μm) is used in this adjustment, Lissajous waves in the initial state may be slightly distorted in the Y-axis direction due to the difference in track pitch. Perform the adjustment for the best point with the GGV1002 (1.52μm).

Note 2 : After adjustment is complete, be sure to perform "17. FOCS gain adjustment" and "18. TRKG servo loop gain adjustment".



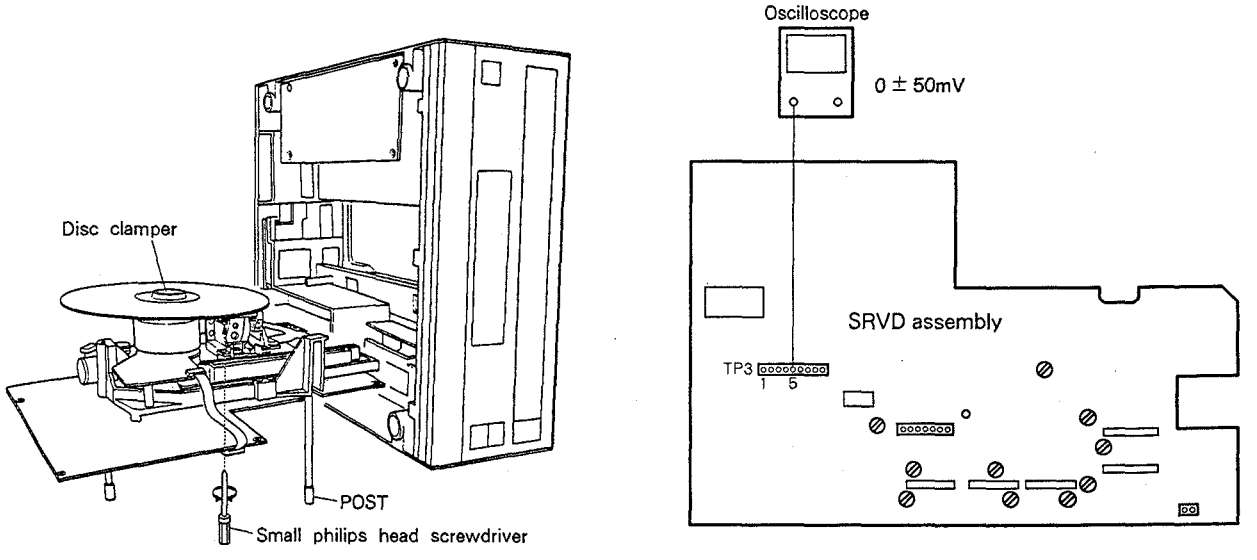
14. Tilt Sensor Inclination Adjustment

Mechanism Adjustment

● Purpose : To adjust the inclination of the tilt sensor optimally (parallel to the disc) so that the LED of tilt sensor light vertically to the disc superficial.
● When not properly adjusted : Crosstalk will be generated.

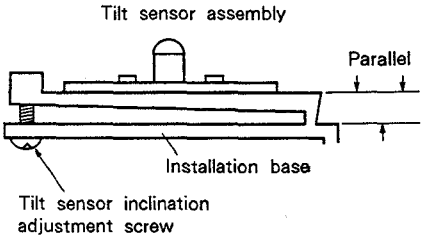
● Measuring instruments and jigs	● Test disc (GGV1002) ● Small philips head screwdriver ● POST ● Disc clamper ● Oscilloscope
● Measuring point	● SRVD assembly TP3-5 (TILT ERR)
● Test disc and player mode	● #115 still ● Test mode : Tilt servo OFF (CX 4), TRKG Servo close (CX 2)
● Position to be adjusted	● Tilt sensor inclination adjustment screw

Connection diagram



Adjustment procedure

1. Check that the tilt sensor assembly is set parallel to the installation base.
2. Play the test disc and search frame #115.
3. Connect TP3-5 in the SRVD assembly to the oscilloscope, and adjust the tilt sensor inclination adjustment screw so that the voltage of TP3-5 becomes 0V ± 50mV.
   Note : At this time, be careful for the other light is not lighted to the tilt sensor.
4. Turn the tilt servo ON by pressing the CX and 5 keys, search frame #115 (STILL mode) and check that the crosstalk is reduced.



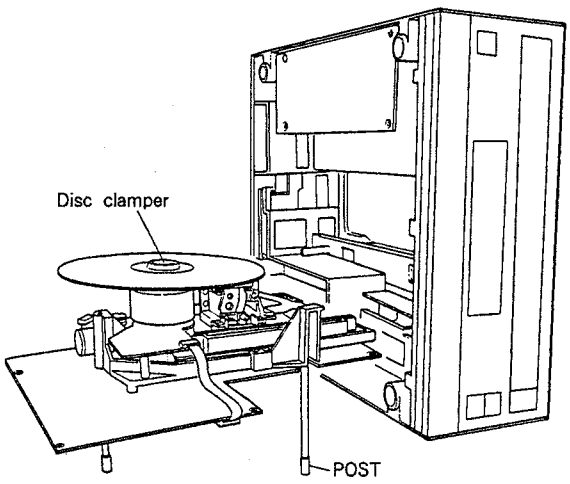
15. RF Level Adjustment

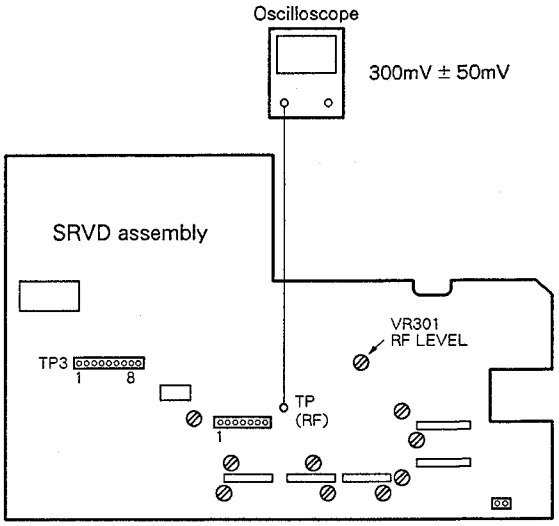
● Purpose : To adjust the level of the RF signal to the optimum value.

● When not properly adjusted : Dropout occurs frequently.

● Measuring instruments and jigs	● Oscilloscope ● POST ● Disc clamper
● Measuring point	● SRVD assembly TP (There is no TP No. "TP (RF)" marked on the P. C. board.)
● Test disc and player mode	● #15,000 still ● Normal mode
● Position to be adjusted	● SRVD assembly VR301

Connection diagram





Adjustment procedure

1. Play the test disc and search frame #15,000.
2. Connect TP (RF signal) in the SRVD assembly to the oscilloscope and observe the RF signal.
3. Adjust VR301 in the SRVD assembly so that the amplitude of the RF signal becomes 300mV ± 50mV.

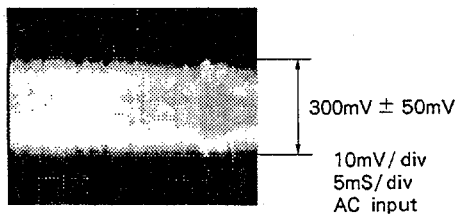


Photo 9 RF signal

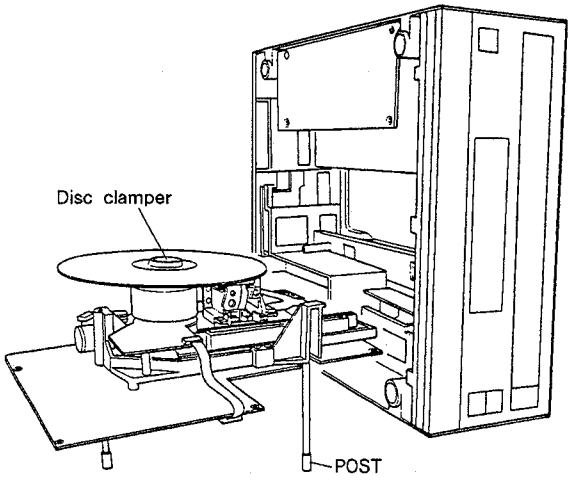
16. Silent FOCS Adjustment

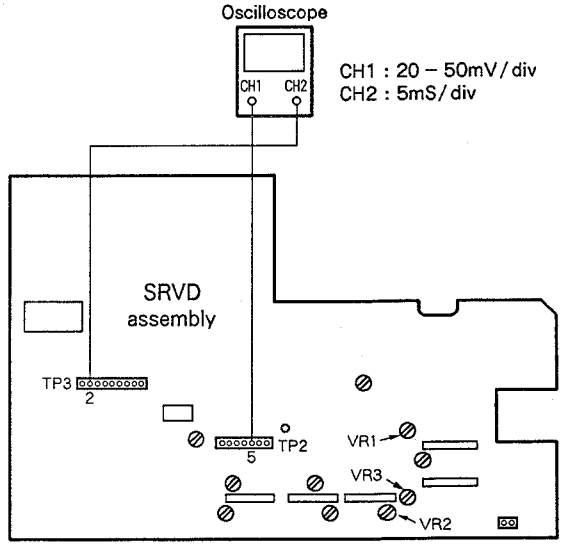
● Purpose : To adjust the TRKG servo components leakage to the FOCS servo becomes minimum.

● When not properly adjusted : When FOCS servo is ON, noise is generated.

● Measuring instruments and jigs	● Oscilloscope ● Test disc (GGV1002) ● POST ● Disc clamper
● Measuring point	● SRVD assembly TP2-5 (FOCS ERR), TP3-2 (TRKG ERR)
● Test disc and player mode	● Around #15,000 ● Test mode ● TRKG servo open
● Position to be adjusted	● SRVD assembly VR1, VR2, VR3

Connection diagram

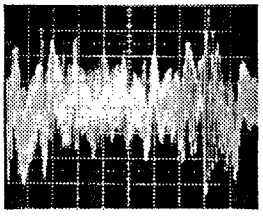




Adjustment procedure

1. Set the player to the test mode.
2. Connect TP2-5 in the SRVD assembly to the CH1 of the oscilloscope and TP3-2 to the CH2.
3. Play the test disc and search frame #15,000, then open the TRKG servo.
4. Trigger the CH2 (TP3-2) of the oscilloscope and observe the waveform of the CH1 (TP2-5).
5. Adjust VR1, VR2 and VR3 in the SRVD assembly so that the waveform of the CH1 (TP2-5) becomes optimum (High-frequency element becomes minimum).

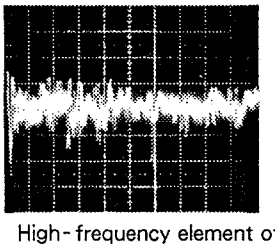
Note 1 : Adjust VR1 through VR3 in no special order.
Note 2 : After adjustment is complete, be sure to perform "17. FOCS gain adjustment".



20 – 50mV/div
5mS/div

High-frequency element of the FOCS error maximum

⇩



High-frequency element of the FOCS error minimum

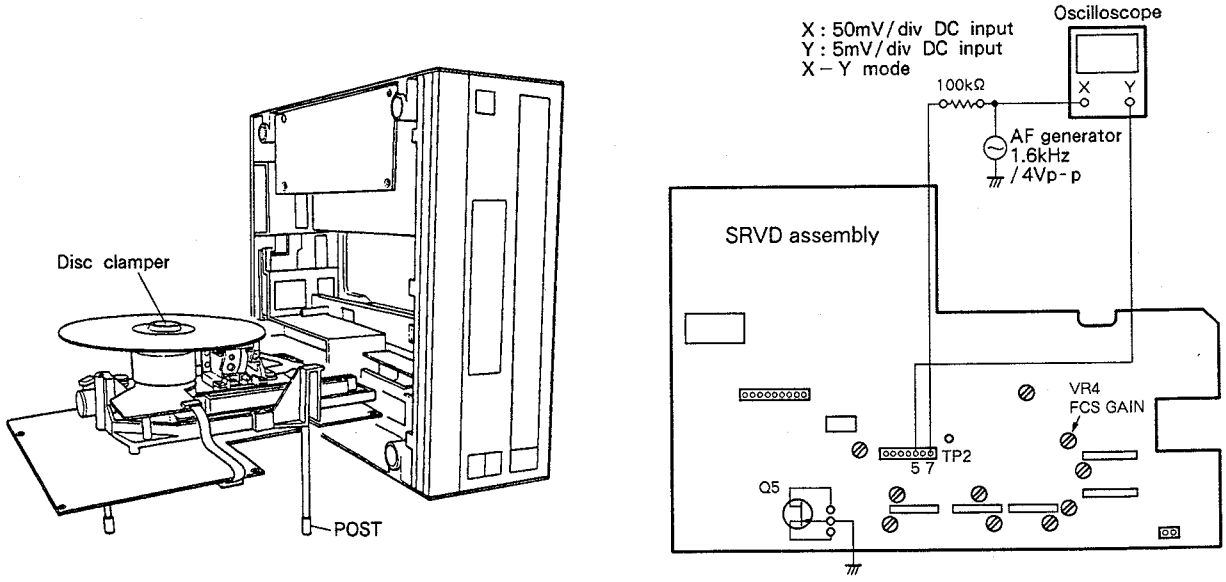
17. FOCS Gain Adjustment

● Purpose : To set the loop gain of the FOCS servo to the optimum value.

● When not properly adjusted : Degraded playing ability

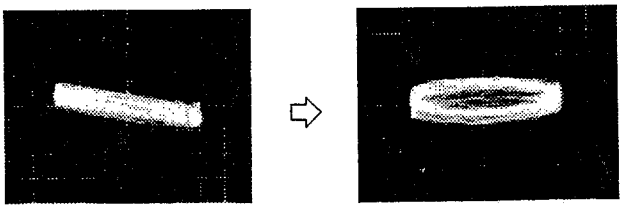
● Measuring instruments and jigs	● Oscilloscope ● AF generator ● Resistor (100kΩ) ● POST ● Disc clamper
● Measuring point	● SRVD assembly TP2-5 (FOCS ERR), TP2-7 (FOCS ERR GAIN)
● Test disc and player mode	● #15,000 still ● FOCS/TRKG servo close
● Position to be adjusted	● SRVD assembly VR4

Connection diagram



Adjustment procedure

1. Connect TP3-7 in the SRVD assembly to GND. (Protection circuit of the FOCS motor is OFF.)
2. Connect TP2-7 in the SRVD assembly to the CH1 (X input) of the oscilloscope via the AF generator and resistor (100k ohms) and TP2-5 to the CH2 (Y input).
3. Search frame #15,000.
4. Set the AF generator output to 1.6kHz/4Vp-p.
5. Adjust VR4 so that the Lissajous figure is symmetrical on both the X- and Y-axes of the oscilloscope.
6. Disconnect TP3-7 to GND.



Adjustment not complete　　Properly adjusted

Photo 10

18. TRKG Servo Loop Gain Adjustment

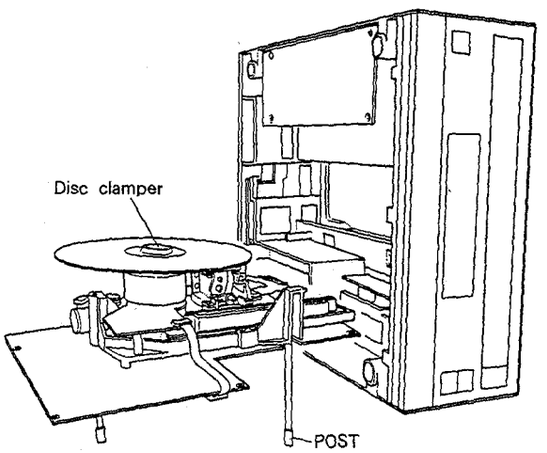
Mechanism Adjustment

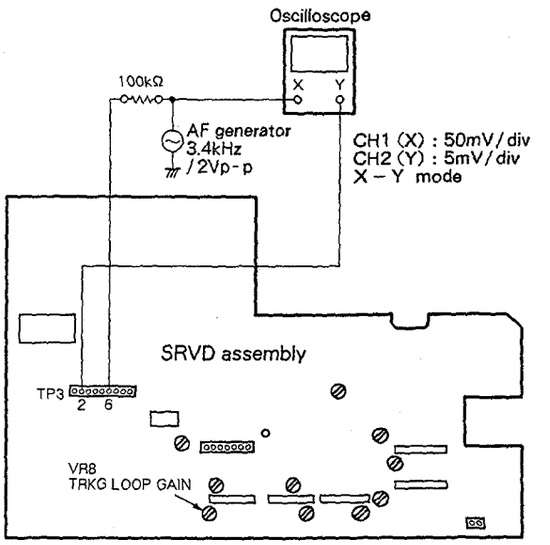
● Purpose : To set the loop gain of the TRKG servo to the optimum value.

● When not properly adjusted : Degraded playing ability.

● Measuring instruments and jigs	● Oscilloscope ● AF generator ● Resistor (100kΩ) ● POST ● Disc clamper
● Measuring point	● SRVD assembly TP3-2 (TRKG ERR), TP3-6 (TRKG ERR GAIN)
● Test disc and player mode	● #15,000 still ● FOCS/TRKG servo close
● Position to be adjusted	● SRVD assembly VR8

Connection diagram



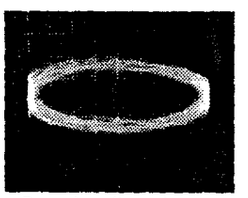


Adjustment procedure

1. Connect TP3-6 in the SRVD assembly to the CH1 (X input) of the oscilloscope via the AF generator and resistor (100k ohms) and TP3-2 to the CH2 (Y input). Set the oscilloscope to the X-Y mode.
2. Search frame #15,000
3. Set the AF generator output to 3.4kHz/2Vp-p.
4. Adjust VR8 so that the Lissajous figure is symmetrical on both the X- and Y-axes of the oscilloscope.

Adjustment not complete

⇩



Properly adjusted

The X-axis and Y-axis of the Lissajous figure are symmetrical.

Photo 11

9.4 ELECTRICAL ADJUSTMENT

9.4.1 SRVD Assembly Adjustment

1. Video Level Adjustment

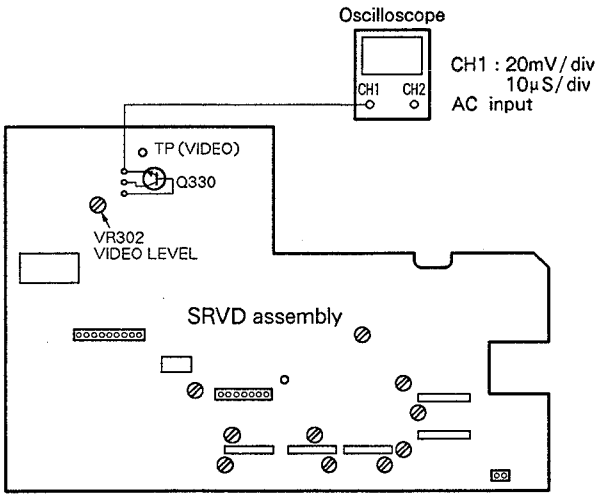
SRVD assembly Adjustment

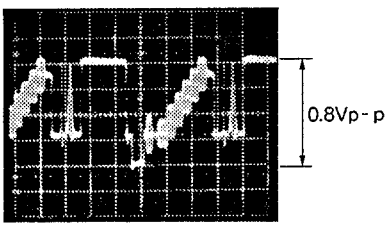
● Purpose : To set the level of the video signal to the optimum value.

● When not properly adjusted : Play starts from the middle of the disc. Screen is too bright or too dark.

● Measuring instruments and jigs	● Oscilloscope ● POST ● Disc clamper
● Measuring point	● Q330 emitter (TP (VIDEO))
● Test disc and player mode	● Test disc GGV1002 #19,801 – #20,700 ● Play mode (Chap. repeat)
● Position to be adjusted	● SRVD assembly VR302

Connection diagram





Adjustment procedure

Note : The video output terminal should be terminated with 75 ohms by connecting to the TV monitor. (When VHF OUT is used for connection to TV, terminate the video output terminal with a 75-ohm resistor.)

1. Play the test disc and search frame #19,801.
2. Adjust VR302 so that the amplitude between the sync tip and the white peak level of the video signal becomes 0.84V – 0.76V.

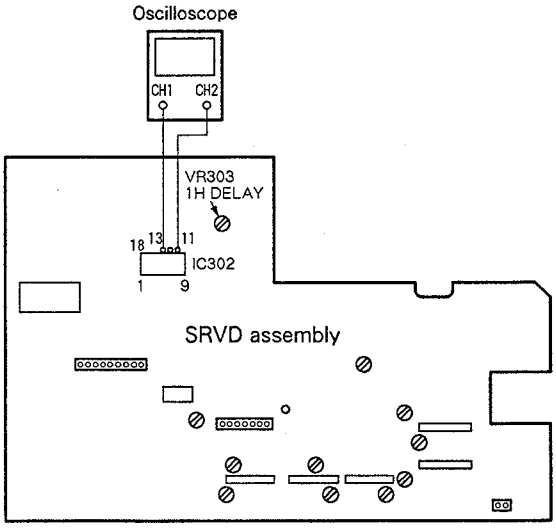
2. 1H Delay Video Level Adjustment

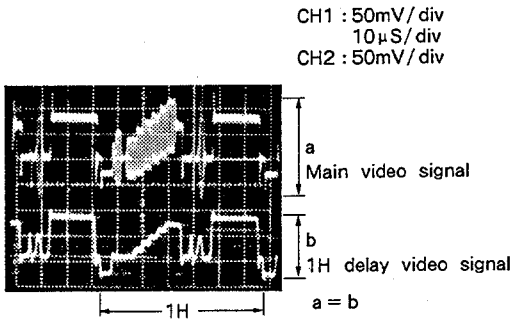
SRVD assembly Adjustment

● Purpose : To adjust the main video signal so that it is equal to the 1H delay video signal.
● When not properly adjusted :
1H delay video is too high → White dropout becomes noticeable and horizontal sync is disordered.
1H delay video is too low → Black dropout becomes noticeable.

● Measuring instruments and jigs	● Oscilloscope ● POST ● Disc clamper
● Measuring point	● SRVD assembly IC302 (PA3018) Pin 11 (CH2), Pin 13 (CH1)
● Test disc and player mode	● Test disc GGV1002 (#3,800, still)
● Position to be adjusted	● SRVD assembly VR303

Connection diagram





Adjustment procedure

1. Play the test disc and search frame #3,800.
2. Connect CH2 and CH1 of the oscilloscope to pin 11 (1H delay side) and pin 13 (main side) of IC302 (PA3018).
3. Adjust VR303 so that the 1H delay video level (CH2) is the same level as the main video level (CH1).

Note : The video level indicates the difference in level between the sync tip level and the white peak level.

9.4.2 CONT Assembly Adjustment

1. Decoder Clock Adjustment

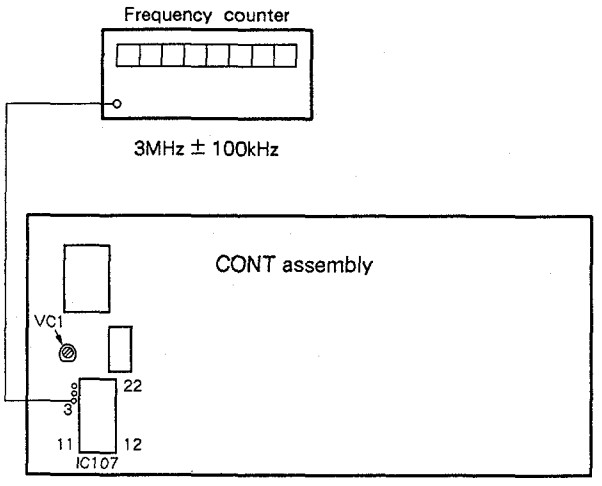
CONT Assembly Adjustment

● Purpose : To set the clock frequency of the decoder to the optimum value.

● When not properly adjusted : Search time is too long.

● Measuring instruments and jigs	● Frequency counter
● Measuring point	● CONT assembly IC107 (PD0011A) Pin 3
● Test disc and player mode	● Test mode PD0011A 3MHz oscillation mode ([CX], [6]) ● Standby mode
● Position to be adjusted	● CONT assembly VC1

Connection diagram



Adjustment procedure

1. Set the player to the Test Mode. (See page 96.)
2. If pressing the [CX] and [6] keys of the remote control, pin 3 of IC107 (PD0011A) becomes 3MHz oscillation mode.
3. Connect the frequency counter to pin 3 of IC107 and adjust VC1 so that the frequency becomes 3MHz ± 100kHz.

Note : If the frequency is difficult to read, pin 3 of IC107 will be pulled up to +5V with a resistor (1k ohms).

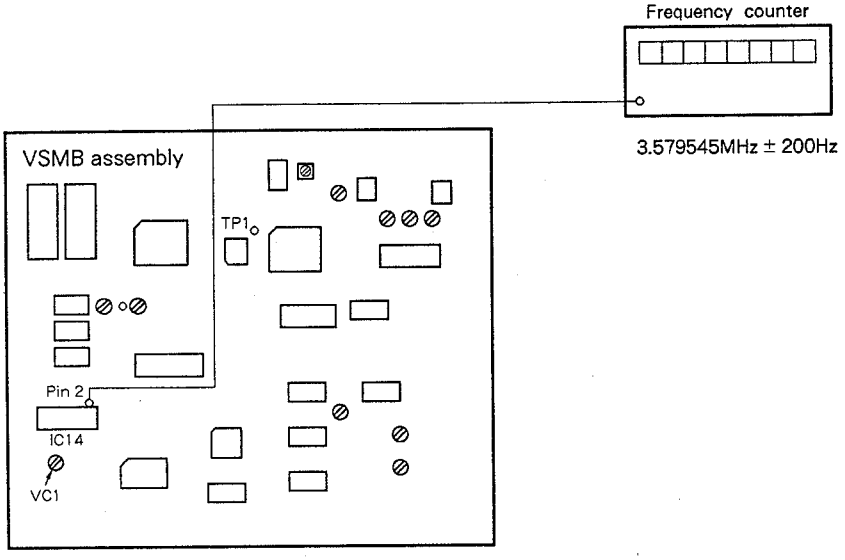
9.4.3 VSMB Assembly Adjustment

1. Master Clock Adjustment

● Purpose : To set the reference clock to the optimum value.

● Measuring instruments and jigs	● Frequency counter
● Measuring point	● VSMB assembly IC14 (TC9015) pin 2
● Test disc and player mode	● Turn POWER switch ON
● Position to be adjusted	● VSMB assembly VC1

Connection diagram



Adjustment procedure

1. Turn the POWER switch ON.
2. Connect the frequency counter to IC14 (TC9015) pin 2 in the VSMB assembly and measure the frequency.
3. Adjust VC1 in the VSMB assembly so that the frequency becomes 3.579545MHz ± 200Hz.

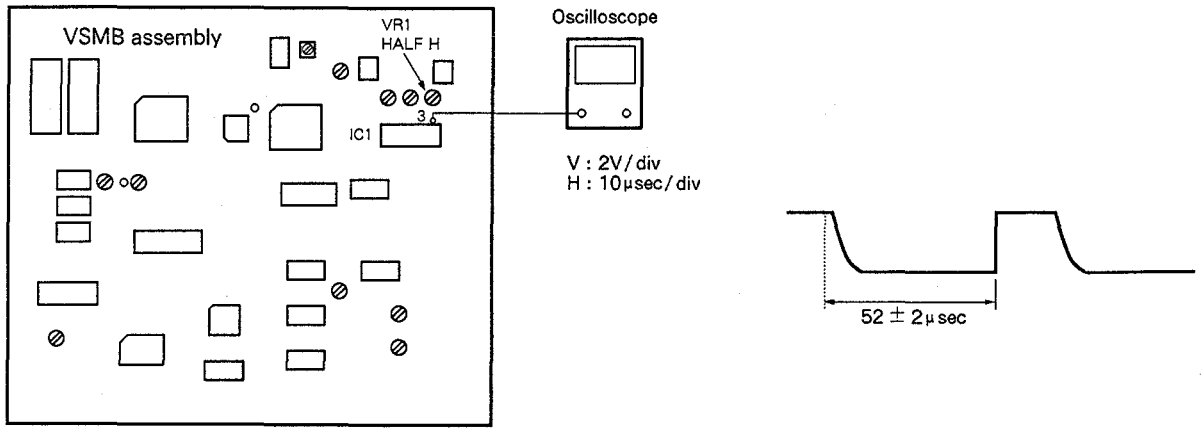
2. Half H Rejection Adjustment

● Purpose : To set the MMV (Monostable Multi Vibrator) output for half H rejection to the optimum value.

● When not properly adjusted : Search time is too long. Picture distored (spindle lock failure).

● Measuring instruments and jigs	● Oscilloscope
● Measuring point	● VSMB assembly IC1 (PA5012) Pin 3
● Test disc and player mode	● LD test disc PLAY
● Position to be adjusted	● VSMB assembly VR1

Connection diagram



Adjustment procedure

1. Play an LD test disc. Connect the oscilloscope to pin 3 of IC1 (PA5012) in the VSMB assembly and observe the pulse waveform.
2. Adjust VR1 in the VSMB assembly so that the pulse width of pin 3 becomes 52 ± 2μsec.

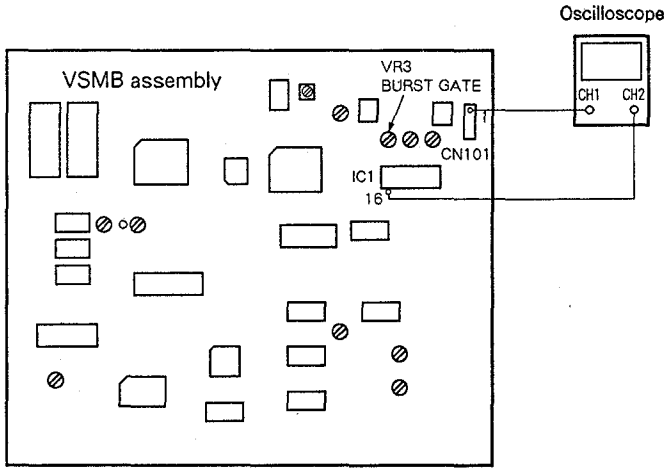
3. Burst Gate Timing Adjustment

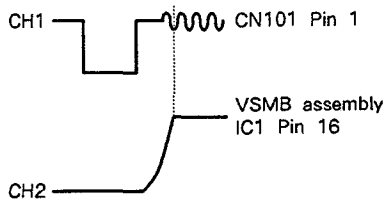
● Purpose : To set the burst gate to the optimum position.

● When not properly adjusted : Playback commenced from intermediate position (not from start of disc), missing or irregular color, fine stripes.

● Measuring instruments and jigs	● Oscilloscope
● Measuring point	● VSMB assembly IC1 (PA5012) Pin 16, CN101 Pin 1
● Test disc and player mode	● LD test disc PLAY
● Position to be adjusted	● VSMB assembly VR3

Connection diagram





First wave of the video burst signal at pin 1 of CN101 and the rising edge of the pulse at pin 16 of IC1 are same timing.

Adjustment procedure

1. Play the LD test disc and set to the still mode.
2. Connect the CH1 of the oscilloscope to pin 1 of CN101 in the VSMB assembly and CH2 to pin 16 of IC1 (PA5012).
3. Adjust VR3 so that the rising edge of the pulse at pin 16 of IC1 and the first wave of the video burst signal at pin 1 of CN101 becomes same timing.

4. VCO Offset Voltage Adjustment

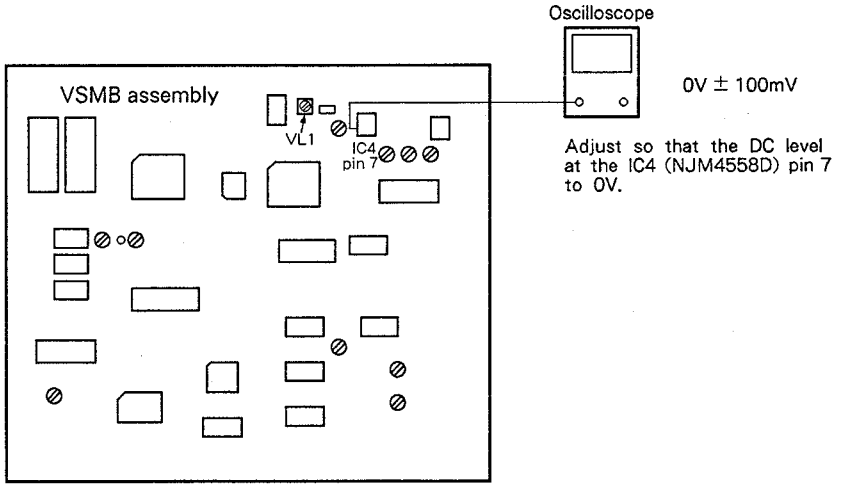
VSMB Assembly Adjustment

● Purpose : To adjust the offset voltage of 14.31818MHz VCO to 0V.

● When not properly adjusted : Picture distored when scanning the CLV disc.
Distortion at H rate. Unstable color

● Measuring instruments and jigs	● Oscilloscope
● Measuring point	● VSMB assembly lead wire of IC4 (NJM4558D) pin 7
● Test disc and player mode	● LD test disc PLAY (PLL lock mode)
● Position to be adjusted	● VSMB assembly VL1

Connection diagram



Adjustment procedure

1. Play the LD test disc.
2. Connect the oscilloscope to IC4 (NJM4558D) pin 7 in the VSMB assembly.
3. Adjust VL1 so that the DC level at the lead wire of R29 becomes 0V ± 100mV.

Note : If the DC level is shifted of full width, disc play impossible.

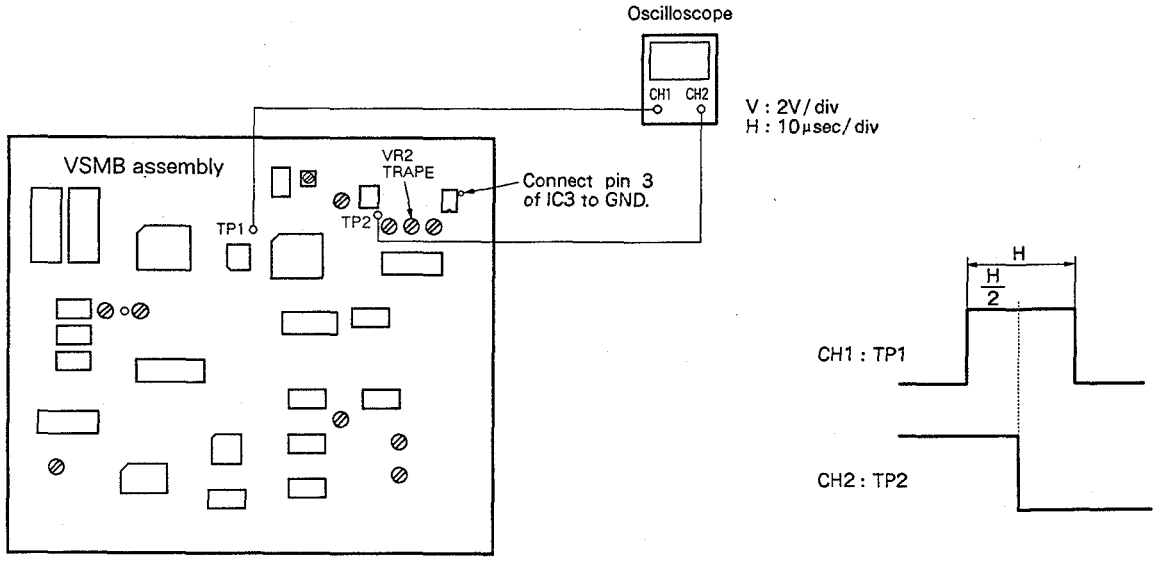
5. Trapezoid Inclination Adjustment

VSMB Assembly Adjustment

● Purpose : To adjust the inclination of the trapezoidal (pulse) waveform used for SPDL and TBC error detection.
● When not properly adjusted : When a CAV disc is used with through-mode, the picture on the screen flickers in the still mode, or the position of the image stored in memory appear in a different position.

● Measuring instruments and jigs	● Oscilloscope
● Measuring point	● VSMB assembly TP1, TP2
● Test disc and player mode	● LD test disc PLAY (PLL lock state) ● VSMB assembly Connect pin 3 of IC3 (DC reset mode)
● Position to be adjusted	● VSMB assembly VR2

Connection diagram



Adjustment procedure

1. Play the test disc and check that the picture on the screen is normal.
2. Connect pin 3 of IC3 to GND in the VSMB assembly. (DC reset mode)
3. Connect TP1 in the VSMB assembly to the CH1 of the oscilloscope and TP2 to the CH2.
4. Adjust VR2 so that the falling edge of the pulse at TP2 is in the center of the H duration at TP1.

6. PLL Gain Adjustment

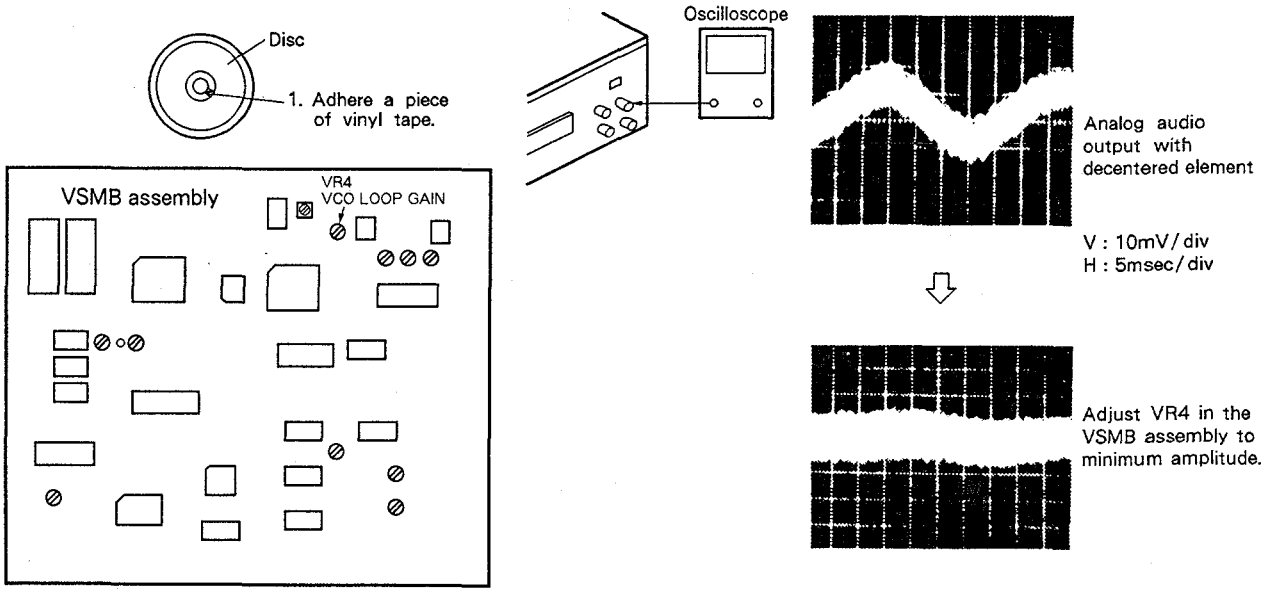
VSMB Assembly Adjustment

● Purpose : To cancel the decentered element on the audio signal.

● When not properly adjusted : Audio SN ratio is degraded. Irregular color significant.

● Measuring instruments and jigs	● Oscilloscope ● Vinyl tape
● Measuring point	● Audio output terminal L and R
● Test disc and player mode	● LD test disc ····· #2,701 (#2,701) ; (Adhere a piece of vinyl tape on the center hole of the disc.)
● Position to be adjusted	● VSMB assembly VR4

Connection diagram



Adjustment procedure

1. Have the LD test disc decentered by adhering a piece of vinyl tape on the center hole of the LD test disc.
2. Connect the oscilloscope to the audio output terminal.
3. Play the LD test disc and search frame #2,701 (#2,701), then observe the waveform.
4. Adjust VR4 in the VSMB assembly so that the amplitude of the waveform and the difference in level between L ch and R ch are minimum.

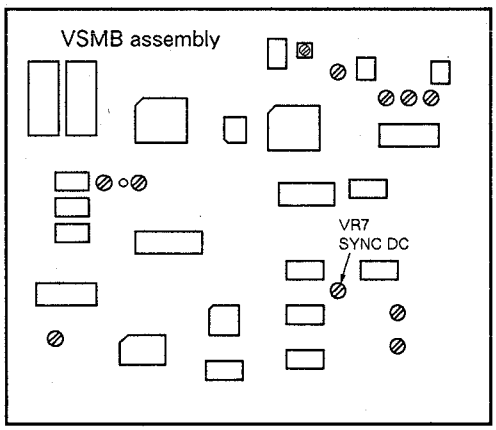
7. Sync DC Level Adjustment

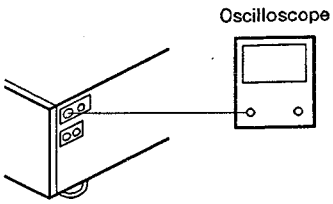
● Purpose : To set the pedestal level of the output video signal to the optimum value.

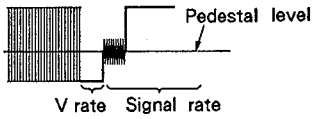
● When not properly adjusted : Screen is too dark or too bright.

● Measuring instruments and jigs	● Oscilloscope
● Measuring point	● Video output terminal
● Test disc and player mode	● LD test disc N-series·····#2,701 (F-series·····#2,701)
● Position to be adjusted	● VSMB assembly VR7

Connection diagram







Adjustment procedure

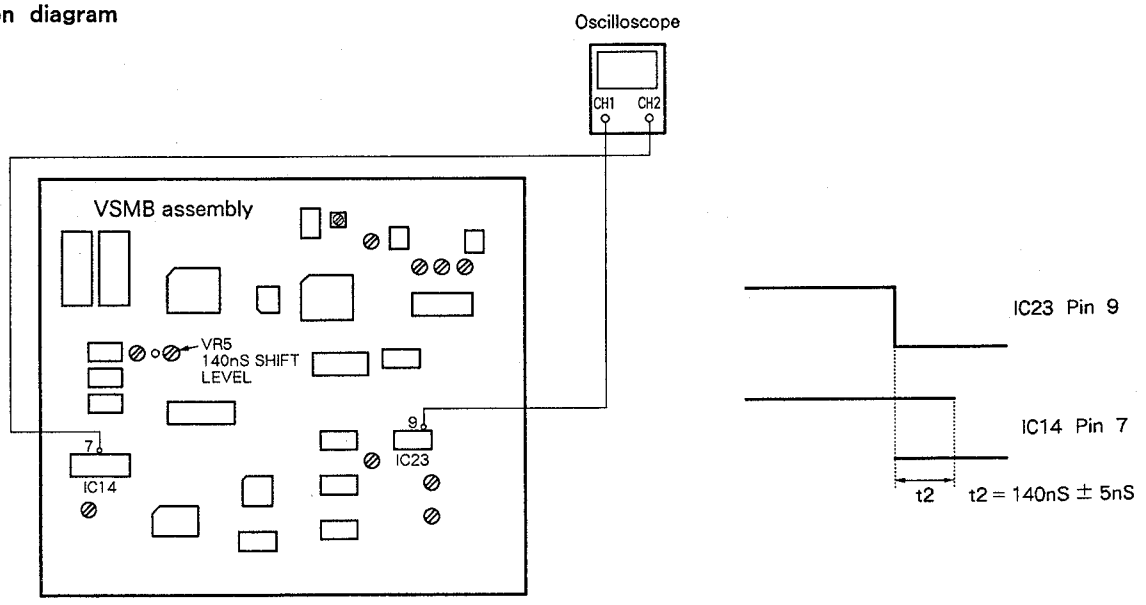
1. Connect the oscilloscope to the video output terminal.
2. Play the LD test disc and search frame #2,701 (#2,701), then observe the video signal waveform by V-rate of the oscilloscope.
3. Adjust VR7 in the VSMB assembly so that the pedestal level of the V-rate and signal rate become continuation.

8. 140 ns Shift Level Adjustment

● Purpose : To set the amplitude of the chroma signal waveform of the video signal which is shifted by 140 ns to the same amplitude as that of the chroma signal waveform of the video signal which is not shifted.
● When not properly adjusted : TV screen flickers.

● Measuring instruments and jigs	● Oscilloscope
● Measuring point	● VSMB assembly IC23 (TC74HC4053AP) Pin 9, IC14 (TC9015P) Pin 7
● Test disc and player mode	● LD test disc N-series……#7,201 (F-series……#6,301)
● Position to be adjusted	● VSMB assembly VR5

Connection diagram



Adjustment procedure

1. Connect pin 9 of IC23 in the VSMB assembly to the CH1 of the oscilloscope and pin 7 of IC14 to the CH2.
2. Play the LD test disc and search frame #7,201 (#6,301).
3. Trigger the oscilloscope at the falling edge of the output pulse from pin 9 (CH1) of IC23.
4. Adjust VR5 in the VSMB assembly so that t2 in the figure becomes 140nS ± 5nS.

9. C Level Adjustment

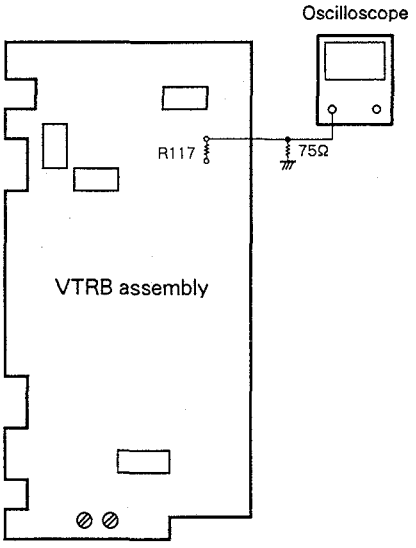
VSMB Assembly Adjustment

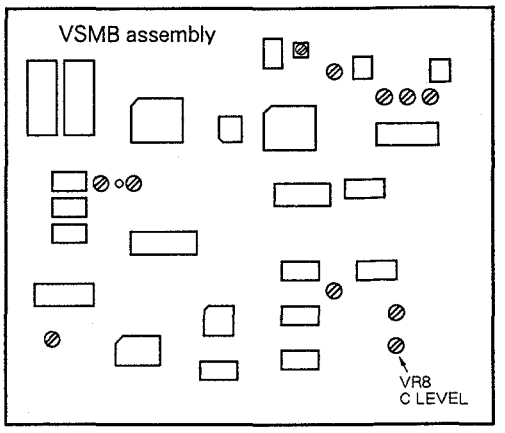
● Purpose : To set the burst level of the video signal to the optimum value.

● When not properly adjusted : Irregular color significant.

● Measuring instruments and jigs	● Oscilloscope ● Test disc ● Resistor (75Ω)
● Measuring point	● VTRB assembly Lead wire of R117
● Test disc and player mode	● Test disc #19,801 still
● Position to be adjusted	● VSMB assembly VR8

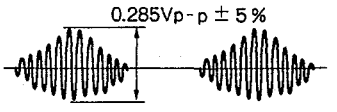
Connection diagram

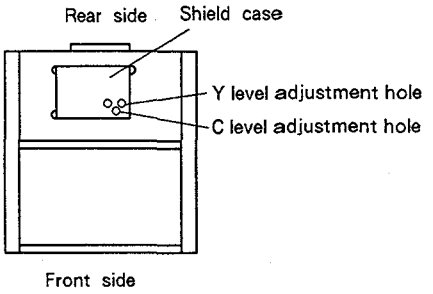




Adjustment procedure

1. Connect the oscilloscope to the lead wire of R117 in the VTRB assembly via the resistor (75-ohm).
2. Play the test disc and search frame #19,801.
3. Observe the burst waveform and adjust VR8 in the VSMB assembly so that the burst level becomes 0.285Vp-p ± 5 %.





10. Y Level Adjustment

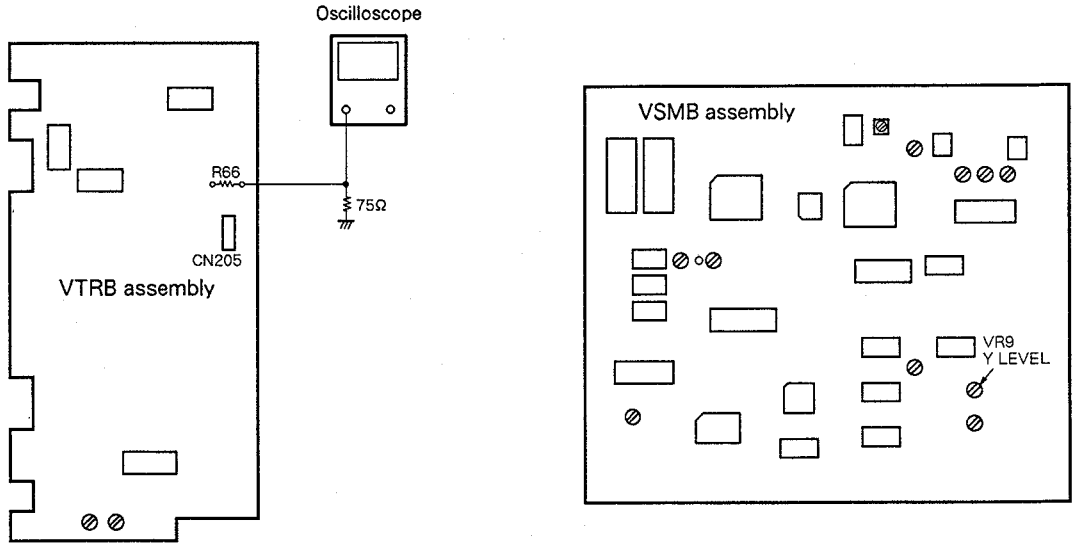
VSMB Assembly Adjustment

● Purpose : To set the luminance level of the video signal to the optimum value.

● When not properly adjusted : Screen is too dark or too bright.

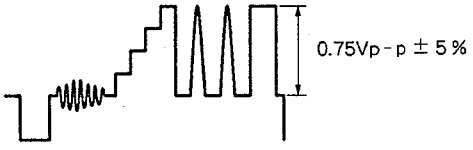
● Measuring instruments and jigs	● Oscilloscope ● Test disc ● Resistor (75Ω)
● Measuring point	● VTRB assembly Lead wire of R66
● Test disc and player mode	● Test disc #19,801 still
● Position to be adjusted	● VSMB assembly VR9

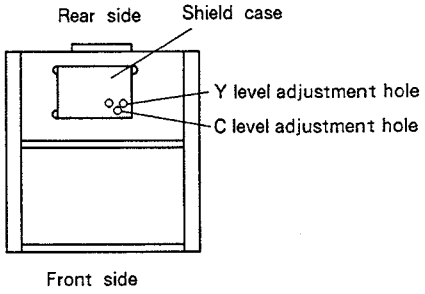
Connection diagram



Adjustment procedure

1. Connect the oscilloscope to the lead wire of R66 in the VTRB assembly via the resistor (75-ohm).
2. Play the test disc and search frame #19,801.
3. Observe the video signal waveform and adjust VR9 in the VSMB assembly so that the luminance level becomes 0.75Vp-p ± 5%.





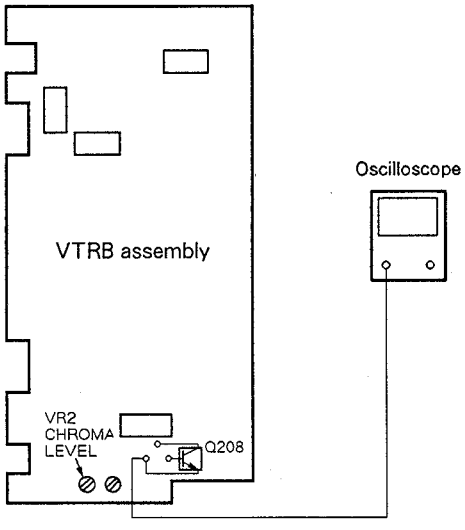
9.4.4 VTRB Assembly Adjustment

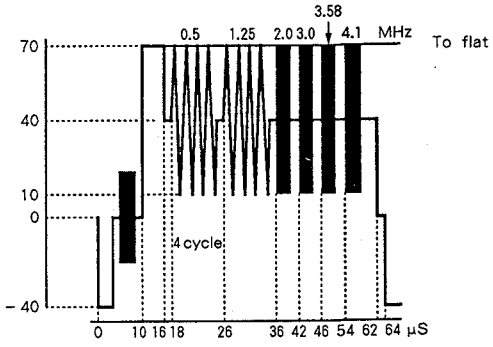
1. Chroma Level Adjustment

● Purpose : To set the signal level of each frequency bands to the optimum value.

● Measuring instruments and jigs	● Oscilloscope ● Test disc
● Measuring point	● VTRB assembly Q208 Emitter
● Test disc and player mode	● Test disc #901 still
● Position to be adjusted	● VTRB assembly VR2

Connection diagram





Multi-burst (70 %)

Adjustment procedure

1. Connect the oscilloscope to the emitter of Q208 in the VTRB assembly.
2. Play the test disc and search frame #901 (multi-burst).
3. Observe the waveform and adjust VR2 in the VTRB assembly so that the level of each frequency bands become flat.

2. Color Phase Error Signal Level Adjustment

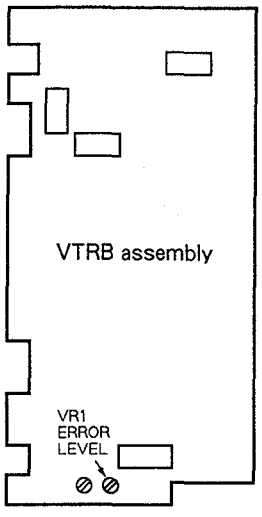
VTRB Assembly Adjustment

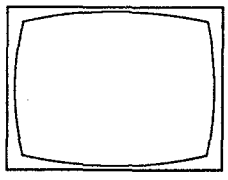
● Purpose : To set the amount of the color phase error signal applied to the color phase compensation section to the optimum value.

● When not properly adjusted : Color shade (irregular color) significant.

● Measuring instruments and jigs	● TV monitor
● Measuring point	● Adjust by watching the screen of the monitor.
● Test disc and player mode	● LD test disc N-series……#7,201 (F-series……#26,101) magenta screen, still
● Position to be adjusted	● VTRB assembly VR1

Connection diagram





Color shading of the magenta screen is minimized.

Adjustment procedure

1. Play the LD test disc and search frame #7,201 (#26,101).
2. Adjust VR1 in the VTRB assembly so that the color shading of the magenta screen is minimized.

9.4.5 DCDR Assembly Adjustment

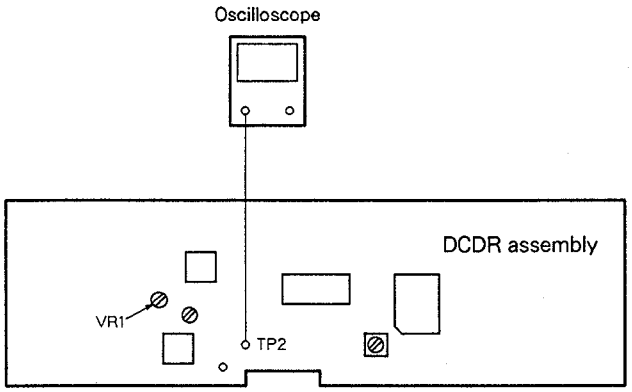
1. VCXO Offset Adjustment

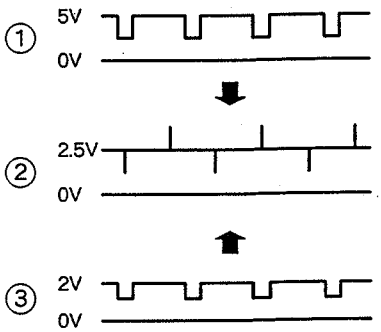
● Purpose : To set the offset voltage of the VCXO PLL phase error signal to minimum.

● When not properly adjusted : Digital audio output is interrupted when playing on LDD disc.
(Noise appears synchronously)

● Measuring instruments and jigs	● Oscilloscope
● Measuring point	● DCDR assembly TP2
● Test disc and player mode	● LDD disc PLAY any frame
● Position to be adjusted	● DCDR assembly VR1

Connection diagram





Adjustment procedure

1. Connect the oscilloscope to TP2 in the DCDR assembly.
2. Play any frame of the LDD disc and observe the waveform of TP2.
3. When the pulse is appeared as shown in figure ① or ③, adjust VR1 so that the positive and negative pulses become nearly equal from the center of 2.5V DC as shown in figure ②.

2. Free-running Frequency Adjustment

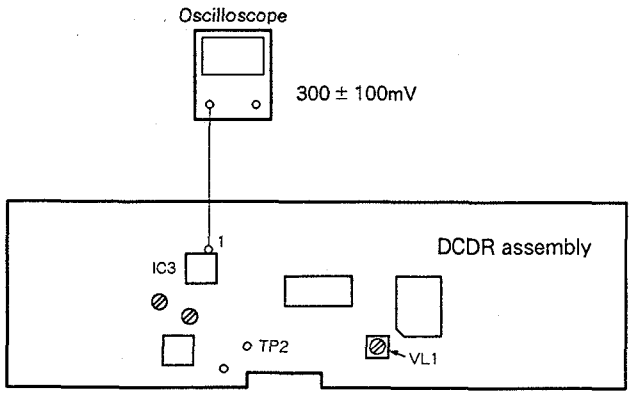
DCDR Assembly Adjustment

● Purpose : To set the VCO free-running frequency for the EFM decoder to the optimum value.

● When not properly adjusted : No sound or sound is interrupted.

● Measuring instruments and jigs	● Oscilloscope
● Measuring point	● DCDR assembly IC3 Pin 1
● Test disc and player mode	● LD disc with digital audio (hereinafter, LDD) PLAY any frame
● Position to be adjusted	● DCDR assembly VL1

Connection diagram



Adjustment procedure

1. Connect the oscilloscope to the pin 1 of IC3 in the DCDR assembly.
2. Play any frame of the LDD disc.
3. Adjust VL1 in the DCDR assembly so that the voltage of IC3 pin 1 becomes 300 ± 100mV.

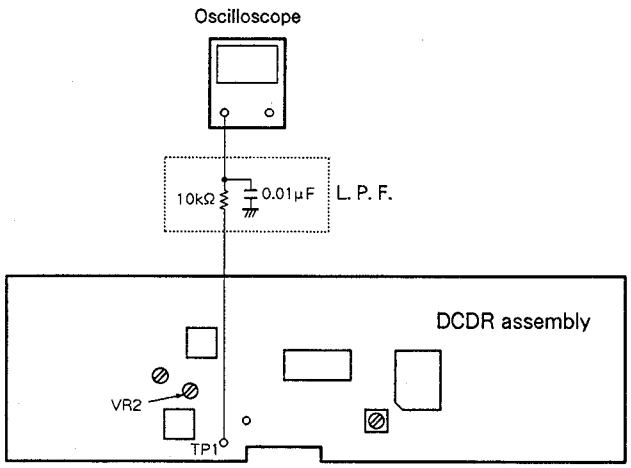
3. VCXO Error Adjustment

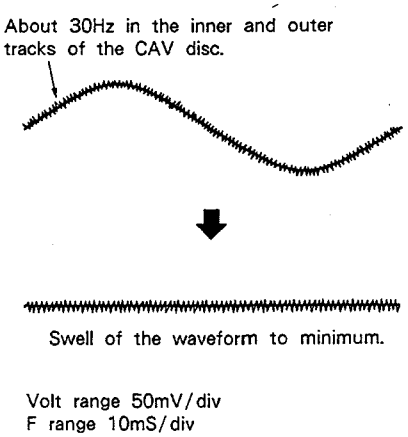
● Purpose : To set the VCXO PLL phase error signal to the optimum value.

● When not properly adjusted : Sound is interrupted when playing on LDD disc.

● Measuring instruments and jigs	● Oscilloscope ● L. P. F (10kΩ resistor, 0.01μF capacitor)
● Measuring point	● DCDR assembly TP1
● Test disc and player mode	● LDD disc (inner track) PLAY
● Position to be adjusted	● DCDR assembly VR2

Connection diagram





Adjustment procedure

1. Play the inner track of the LDD disc.
2. Connect the oscilloscope to TP1 in the DCDR assembly via L. P. F. and observe the waveform.
3. Adjust VR2 in the DCDR assembly so that the swell of the waveform becomes minimum.

9.4.6 DACB Assembly Adjustment

1. MSB Adjustment (Reference)

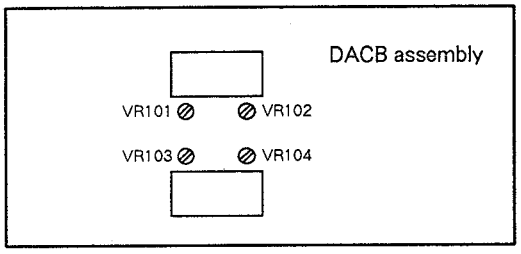
DACB Assembly Adjustment

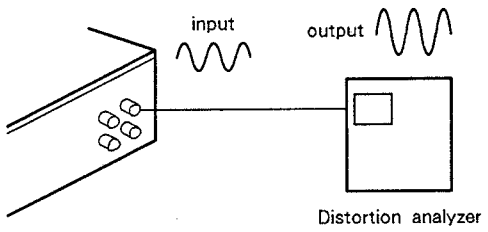
● Purpose : To adjust the distortion of the digital audio signal to minimum.

● When not properly adjusted : Digital audio signal will be distorted.

● Measuring instruments and jigs	● Distortion analyzer
● Measuring point	● Digital audio output terminal
● Test disc and player mode	● M1 test disc chap 2 – 3 (1kHz, 0dB) PLAY
● Position to be adjusted	● DACB assembly VR101, VR102, VR103, VR104

Connection diagram



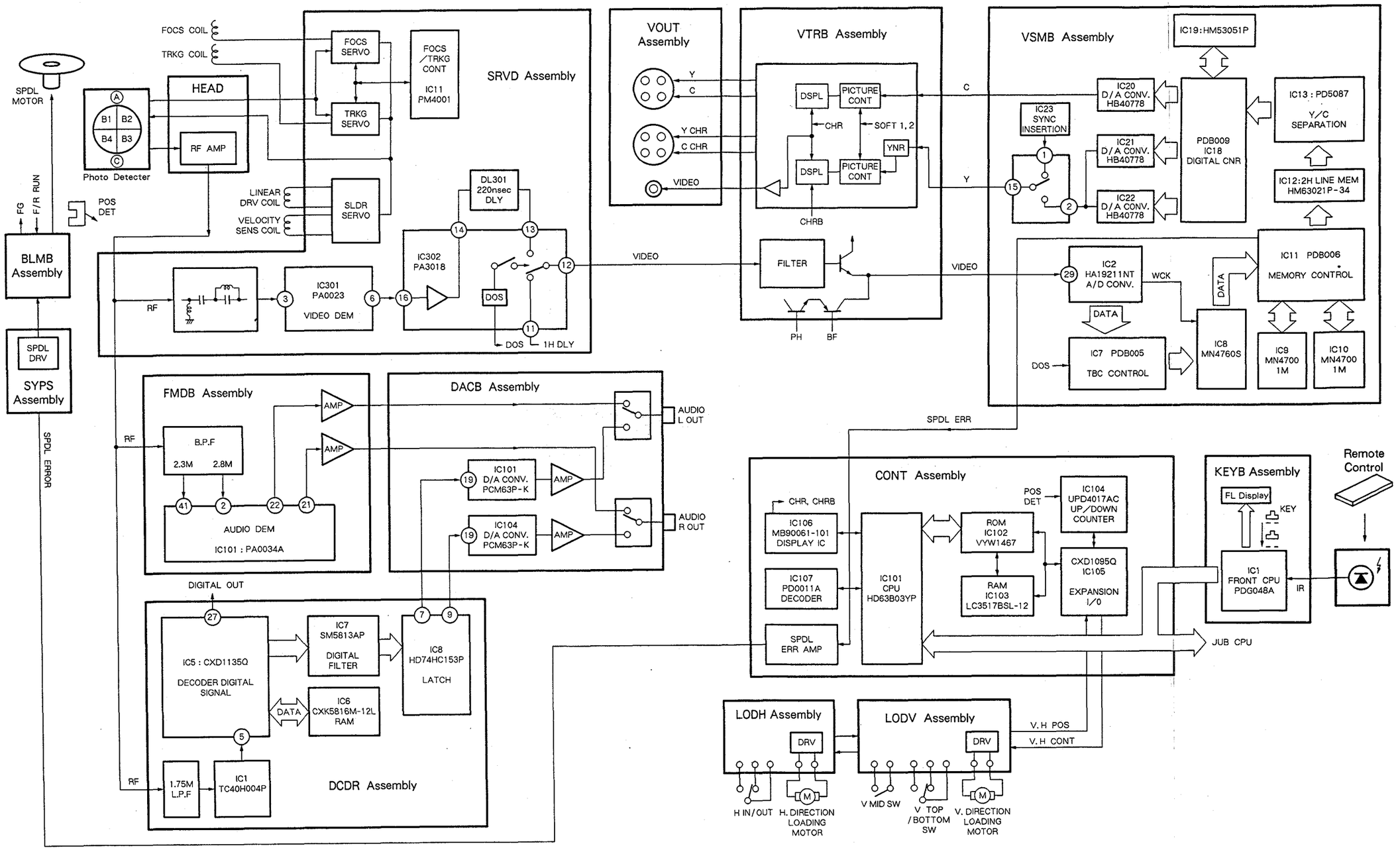


Adjustment procedure

1. Connect the distortion analyzer to the digital audio output terminal.
2. Play the M1 test disc chap 2 (1kHz, 0dB) and set the distortion mode. (20kHz, L. P. F. ON)
3. Adjust VR101 and VR102 (for L ch) so that the distortion factor becomes minimum (0.0018%).
4. Adjust VR103 and VR104 (for R ch) so that the distortion factor becomes minimum.

10. CIRCUIT DESCRIPTION

10.1 OVERALL BLOCK DIAGRAM



10.2 FOCS, TRKG AND SLDR (LINEAR) SERVOS

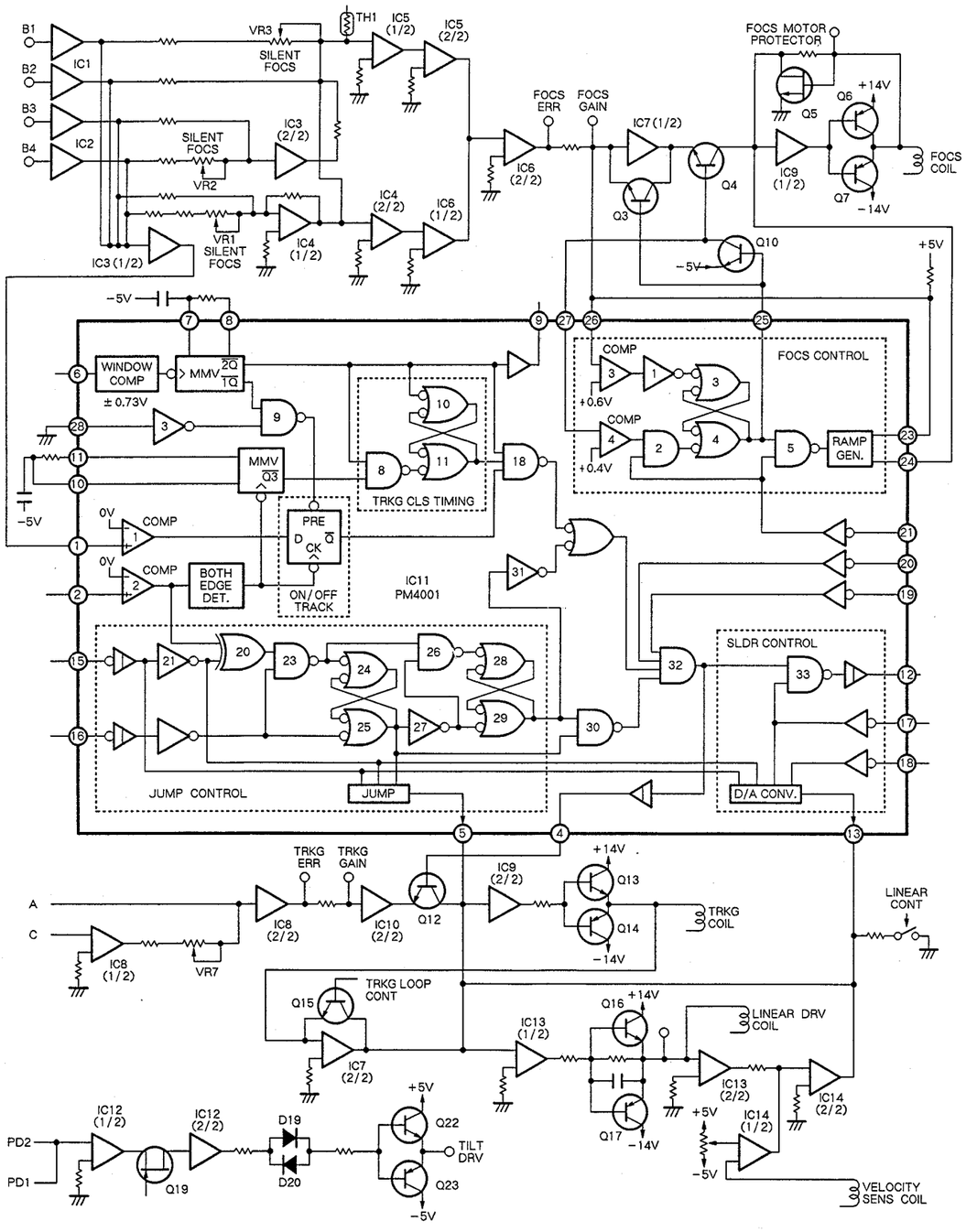


Fig. 10-1 Block diagram of the FOCS, TRKG and SLDR (linear) servos

10.2.1 FOCS, TRKG and SLDR (linear) servo configurations

The focus, tracking and slider servo circuits of the LD-S2 (hereinafter abbreviated to FOCS, TRKG and SLDR respectively) are composed of the HEAD block after the photo detector and the focus coil and tracking coil of the SRVD assembly and pickup block. The block diagram of the FTS block of the SRVD assembly is shown in Fig. 10-1.

10.2.2 Function of the PM4001

The PM4001 is a 28-pin IC which contains both bipolar and PMOS structures. Main functions of the PM4001 in the LD-S2 are as follows.

- UP/DOWN movements of the objective lens upon activation
- Loop SW control of the FOCS servo
- Loop SW control of the TRKG servo
- Power voltage generation to drive the slider for scanning
- Jump pulse generation

Functions of the pins are described below.

Pin 1 ····· FOCS A + B signal input; comparison input for the detected amounts of "ON-TRACK" and "OFF-TRACK" of the MAIN BEAM. The comparison level is the GND level. "ON-TRACK" when COMP1 output is "L".

Pin 2 ····· TRKG error input; comparison input for detected JUST "ON" or "OFF-TRACK" timings of the MAIN BEAM. The comparison level is the GND level.

Pin 3 ····· GND

Pin 4 ····· Loop SW control output of the TRKG servo; open collector output (open or −5V). Loop open at −5V.

Pin 5 ····· JUMP PULSE output; outputs three values of +4V, −4V and 0V.

Pin 6 ····· TRKG STOPPER input; WINDOW COMP input for the stopper. The comparison level is ±0.68V.

Pin 7, Pin 8 ··· Time constant connection terminal for MMV1 and 2

Pin 9 ····· MMV2 output

Pin 10, Pin 11 ··· Time constant connection terminal for MMV3, which is retriggerable and used for frequency detection of TRKG errors.

Pin 12 ··· SLDR LOOP control output; not used in the LD-S2.

Pin 13 ··· SCAN output; voltage output terminal for the slider motor drive.

Pin 14 ··· VEE ; −5V

Pin 15 ··· FWD/$\overline{\text{REV}}$ input (TTL); input terminal to determine the direction of scan and jump operations.

Pin 16 ··· $\overline{\text{JUMP TRIG}}$ input (TTL)

Pin 17 ··· SCAN ON/$\overline{\text{OFF}}$ input (TTL)

Pin 18 ··· SCAN SPEED input (TTL); HIGH SPEED with "L" level

Pin 19 ··· $\overline{\text{TRKG ON}}$ input (TTL); TRKG loop is forcibly opened with "H" level.

Pin 20 ··· DELAYED FOCS LOCK input; TRKG loop close is enabled with "L". (Threshold level ≈2V)

Pin 21 ··· $\overline{\text{FOCS ON}}$ input (TTL)

Pin 22 ··· Vcc ; +5 V

Pin 23 ··· OSC OUT; open collector output (open or −5V); −5V when RAMP is negative and "open" when RAMP is positive and at FOCS OFF and FOCS LOCK.

Pin 24 ··· RAMP OUT; to charge and discharge capacitors by a fixed current. Ramp output of +3V, −2V, 1Hz.

Pin 25 ··· $\overline{\text{FOCS LOCK}}$ output; open collector output (open or −5V), Loop closed at −5V.

Pin 26 ··· FOCS A−B input; comparison input for S-curve waveform detection. The comparison level is +0.6V.

Pin 27 ··· TRKG A+B input; comparison input for DISC detection. The comparison level is +0.4V.

Pin 28 ··· TRKG LOOP input

10.2.3 FOCS servo

(1) STAND-BY state

In STAND-BY state, $\overline{\text{FOCS ON}}$ supplied to pin 21 of IC11 (PM4001) of the SRVD assembly is set to "H" level by IC101 (CPU) of the CONT assembly setting the output from pin 25 ($\overline{\text{FOCS LOCK}}$) of IC11 to "H" and loop switch Q1 to "ON".

(2) Upon INITIAL START

When the unit shifts from STAND-BY state to PLAY mode, the output ($\overline{\text{LD ON}}$) of the CPU (IC101) in the CONT assembly becomes "L" and the laser diode lights. At the same time, the output of NAND GATE5 in the PM4001 becomes "L", suppling RAMP waveforms from pin 24. This RAMP output drives the objective lens. When the lens comes close to the position in which "IN-FOCUS" is possible, the level of the TRKG A + B signal supplied to pin 27 of the PM4001 is increased and the output of the comparator 4 in the PM4001 is inverted from "L" to "H". The FOCS A−B signal supplied to pin 26 of the PM4001 changes to a S curve near the "JUST FOCUS" point. The comparator 3 detects the zero cross point, inverting the output from "L" to "H". At the same time, the F.F. output composed of INV-OR GATE 3 and 4 or the pin 25 output becomes "L" and loop switch Q3 is turned off, closing the FOCS servo loop. Simultaneously, the NAND GATE5 becomes "H" and the RAMP output ends. Fig. 10-2 shows the timing chart of these operations and Fig. 10-3 shows the block diagram relating to FOCS.

(3) Recovery from de-focus

If de-focus occurs due to some reason with the FOCS servo loop closed, the TRKG A ± B signals become 0V and the F.F. output composed of INV-OR GATE 3 and 4 becomes "H", opening the servo loop, and the NAND GATE5 is set to "L". outputting RAMP waveforms from pin 24. The timing chart is shown in Fig. 10-4.

(4) Regular operations

A focus error is generated by operating and amplifying the 4th-dividing photo-detector output at IC1 to IC6 in the SRVD assembly. The error is then amplified by the driver amplifier of IC9 (1/2) via an equalizer composed of IC7 (2/2) in the SRVD assembly and the current is amplified by Q6 and Q7, driving the objective lens. The TH1 (thermistor) is for temperature compensation for the multi-lens.

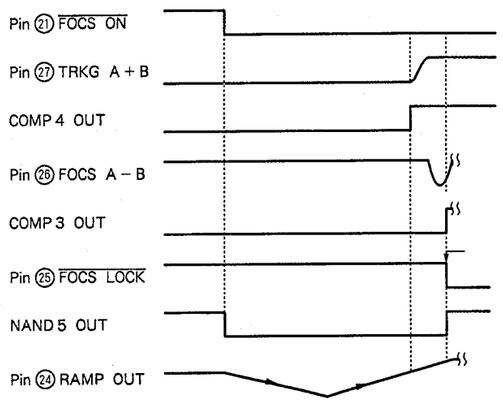


Fig. 10-2 Timing chart at the FOCS is actived

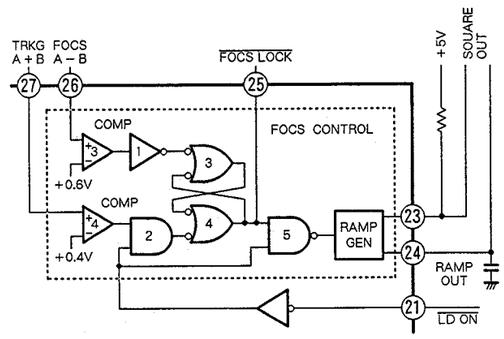


Fig. 10-3 Block diagram relating to FOCS

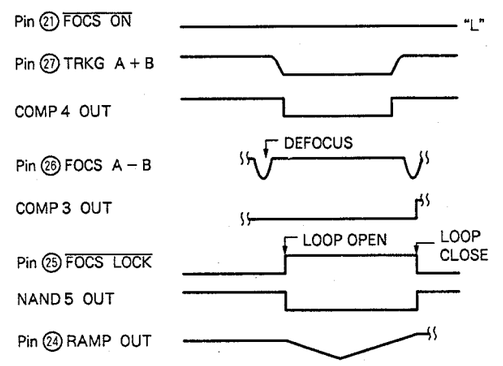


Fig. 10-4 Recovery from de-focus

10.2.4 TRKG servo

(1) STAND-BY state

In the STAND-BY state, pin 19 ($\overline{\text{TRK O/C}}$) and pin 17 (SCAN ON/$\overline{\text{OFF}}$) of IC11 (PM4001) are set to "H". The TRKG and SLDR loops are opened.

(2) TRKG servo upon INITIAL START

When FOCS LOCK is completed, the $\overline{\text{FOCS LOCK}}$ signal (in "L" level) is sent from Q11 to the CPU, which then sets $\overline{\text{TRKG ON}}$ to "L" level. Subsequently, the DELAYD $\overline{\text{FOCS LOCK}}$ signal (pin 20 of the PM4001) becomes "L" and all four inputs of AND GATE32 become "H", closing the TRKG loop.

(3) JUMP operation

When the MAIN BEAM is required to jump tracks for trick play, etc., the LD-S2 instantaneously moves the actuator in the radial direction, letting the beam jump between tracks.

This intertrack jump of the beam spot is controlled by the $\overline{\text{JUMP TRIG}}$ signal and the FWD/$\overline{\text{REV}}$ signal from the CONT assembly (supplied to pin 16 and 15 of the PM4001 respectively). The pattern of the $\overline{\text{JUMP TRIG}}$ signal and the polarity of the FWD/$\overline{\text{REV}}$ signal depend on operation modes. (See the description of the control system.)

The block diagram of the PM4001 relating to jump is shown in Fig. 10-5 and the timing chart of the jump forward operation is shown in Fig. 10-6. The jump forward pulse of +4V is generated at pin 5 of the PM4001 by the jump trigger supplied to pin 16. At the same time, an "L" level signal is output from pin 4 (TRKG $\overline{\text{O}}$/C), which opens the TRKG servo loop. The jump forward pulse is differentiated and amplified by the amplifier in the SRVD assembly, applying a current to the tracking coil and driving the actuator in the radial direction. Consequently, the beam spot crosses tracks. When the zero order spot is positioned in the center between tracks, the jump forward pulse returns to 0V and the actuator is braked by the differential pulse, simultaneously closing the TRKG loop.

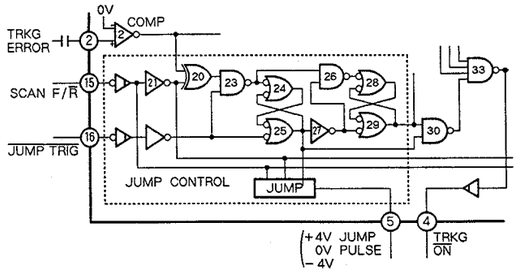


Fig. 10-5 Block diagram relating to jump

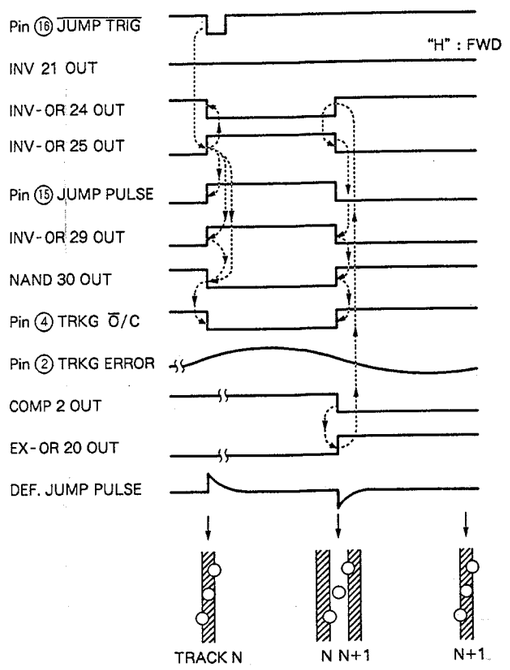
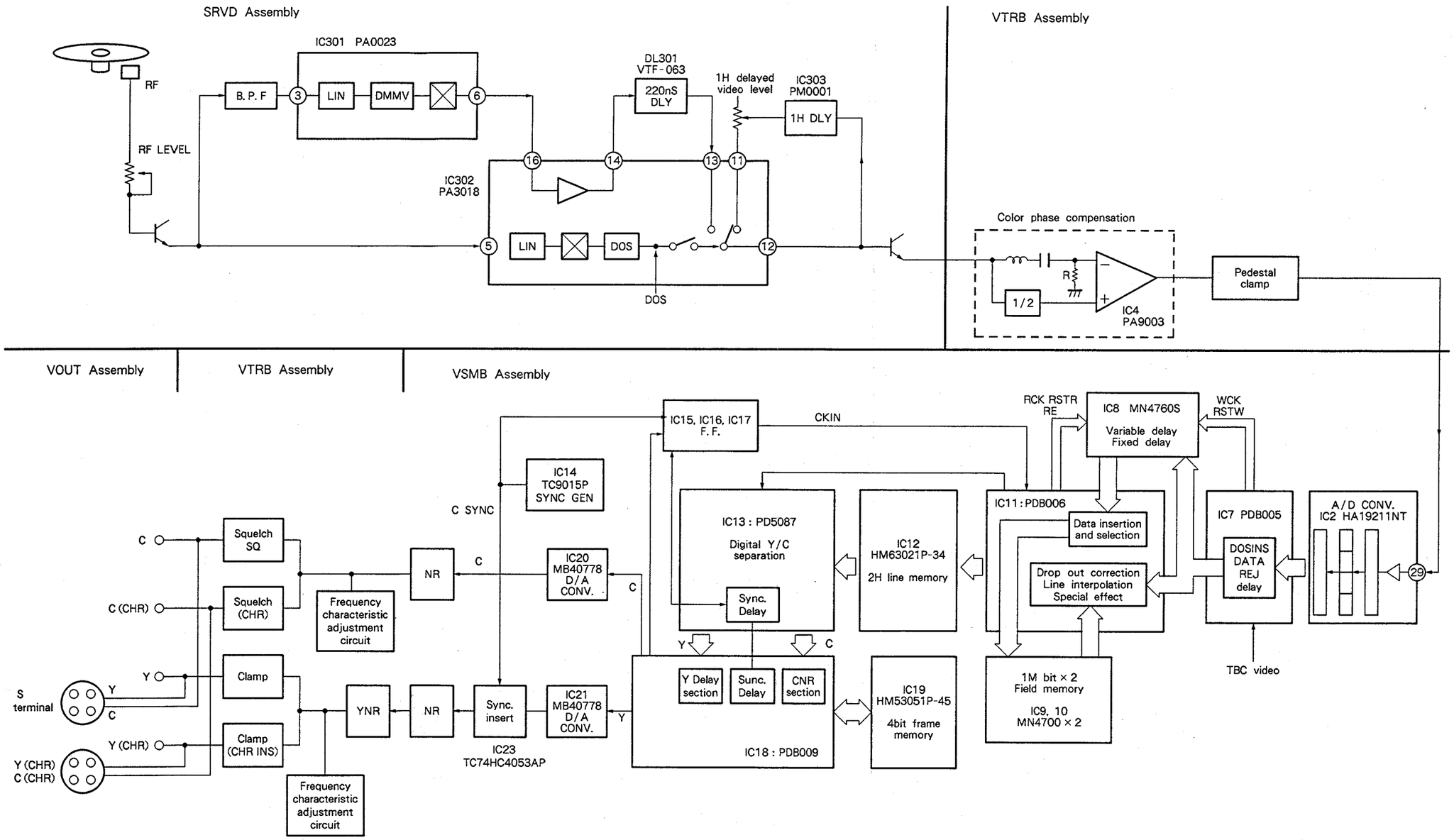


Fig. 10-6 Timing chart of the jump operation

(4) SLDR (linear) servo in regular operations

The TRKG servo loop is closed in play mode. The actuator makes the objective lens trace tracks in the radial direction. However, unless the pickup also moves in the radial direction, the DC component flowing to the tracking coil will gradually increase and finally exceed the traceable range of the actuator. To avoid this, the SLDR (linear) servo in regular operations detects the DC current flowing to the tracking coil and moves the pickup in the radial direction according to the current level so that the actuator always comes to DC-like neutral position.

10.3 VIDEO CIRCUIT DESCRIPTION



10.3.1 Description of the VTRB and VSMB assemblies

Video signals decoded by the SRVD assembly IC302 (PA3018) are divided into the main-track video to be supplied to the VTRB assembly and the TBC video to be supplied to the VSMB assembly. All the analog and digital signal processing operations before the video output terminal are performed on these two circuit boards. The VTRB assembly chiefly performs analog processing and the VSMB assembly chiefly performs digital processing.

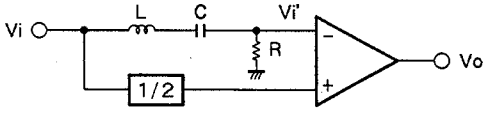
The main-track video signals supplied to the VTRB assembly accept color compensation at the CPCB (Color Phase Compensation Block).

(1) Description of the color phase compensation circuit

The circuit to compensate for color unevenness caused by residual jitter is composed of the differential amplifier in the PA9003 and the phase modulation circuit of Q203, VR2 and L201. The principle diagram of this circuit is shown in Fig. 10-7.

The formulas below defining the input voltage as Vi, the direct input voltage of the differential amplifier as Vi' and the output voltage as Vo indicate that this system provides a phase circuit which changes only the phase without changing the amplitude. Therefore, when variable capacity elements are employed on these capacitors in the figure, they can form a phase conversion circuit.

In the actual circuit, the color compensation is performed by supplying video signals to pin 14 (⊕ input) and the color signal components passed through C204 to pin 15 (⊖input) of the differential amplifier in the PA9003 and driving the reversed bias voltage of VR2 by the residual jitter component. As this phase modulation is done by changing the reversed bias voltage of the variable capacitor, the amplitude of the signal to be modulated (color signal) must be sufficiently smaller than that of the modulation signal (residual jitter) to eliminate distortion. With this color phase compensation, the residual color phase error can be compressed from around 40 to 50°p-p after the CCD to around 8°p-p.



$$Vi' = \frac{R}{j\omega L + \frac{1}{j\omega C} + R} \qquad Vi = \frac{j\omega CR}{(1-\omega^2 LC) + j\omega CR} Vi$$

$$Vo = 2\left\{\frac{1}{2} Vi' - Vi\right\} = 2\left\{\frac{1}{2} - \frac{j\omega CR}{(1-\omega^2 LC) + j\omega CR}\right\} Vi$$

$$F(j\omega) = \frac{Vo}{Vi} = 1 = \frac{2j\omega CR}{(1-\omega^2 LC) + j\omega CR} = \frac{(1+\omega^2 LC) + j\omega CR}{(1-\omega^2 LC) + j\omega CR}$$

$$\therefore |F(j\omega)| = 1 \qquad \angle F(j\omega) = 2\tan^{-1}\frac{-\omega^2 LR}{1-\omega^2 LC}$$

Fig. 10-7
Principle diagram of the color phase compensation circuit

(2) Digital Y/C separation

The color phase compensated video data is sent to the VSMB assembly after pedestal clamp. The data is there converted from analog to digital and written to line memory. The 8-bit video data read from the line memory is then written to the 1-Mbit field memory. Video data read from the VSMB assembly IC11 (PDB006) is divided into 8 bits data by the digital Y/C separator which is composed of IC12 (2H line memory HM63021P-34) and IC13 (PD5087). They are then input to IC18 (PDB009) for colornoise reduction of the field correlation type with IC19 (4-bit frame memory HM53051P), sending NR-processed color data to the digital/analog converter (IC20 : MB40778). As IC19 is a 4-bit IC, it reads and writes data by dividing it into upper and lower blocks. This IC also performs the logic operation required for converting Y into pseudo 9-bit blocks and outputs the Y data delayed for half a sampling cycle and the clock for D/A conversion.

By adding the Y data delayed for half a cycle and the original Y data after converting them in the respective D/A conversion ICs, IC22 and IC21, the interpolating 9-bit 2-pass oversampling is executed. IC23 (TC74HC4053AP) inserts C sync (composite sync) in the Y signal, which then passes through a low-pass filter composed of L19, L20, C114 and C116 and is sent to the VTRB assembly after a level adjustment at VR9.

The C signal is sent to the VTRB assembly after passing through an L.P.F. composed of L16, L17, C101 and C103.

The Y signal sent to the VTRB assembly first passes through the analog Y-NR (Y noise reduction) circuit and then the frequency response adjustment circuit composed of Q15 and Q16 and is input to IC1 (PA9003). Then, it passes through a character insertion circuit and a squelch circuit and becomes Y (with CHR.) of the S output. Y (without CHR.) passes through the frequency response adjustment circuit composed of Q26 and IC2 and then clamp and squelch circuits before becoming an output.

The C signal passes through the same frequency response adjustment circuit to match the delay time with that of Y. Squelch is applied also to the character block of C for the output with characters. The composite output signals are generated by adding the Y/C signals with characters and those without characters at the add circuit composed of Q38 and Q40.

(3) PD5087 (Digital Y/C separation IC)

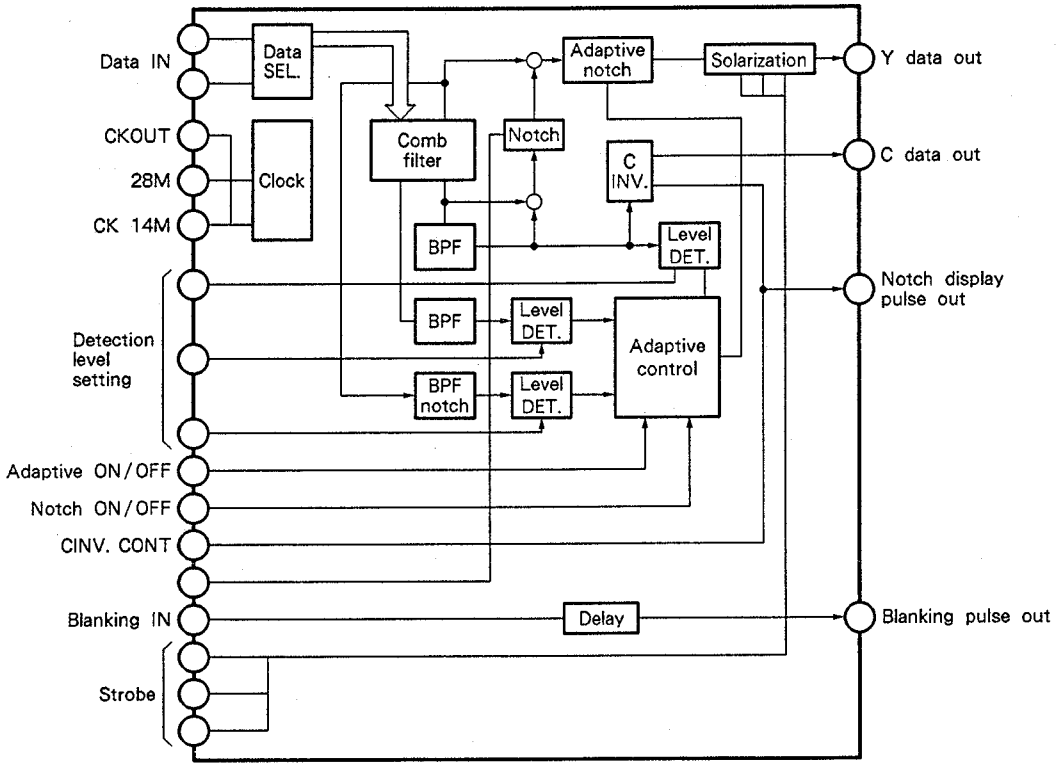


Fig. 10-8 Bloack diagram of the PD5087

The PD5087 is included in the 2H type comb filter. The difference of block diagram and verticfal gain of the 1H type and the 2H type are shown in Fig. 10-9.

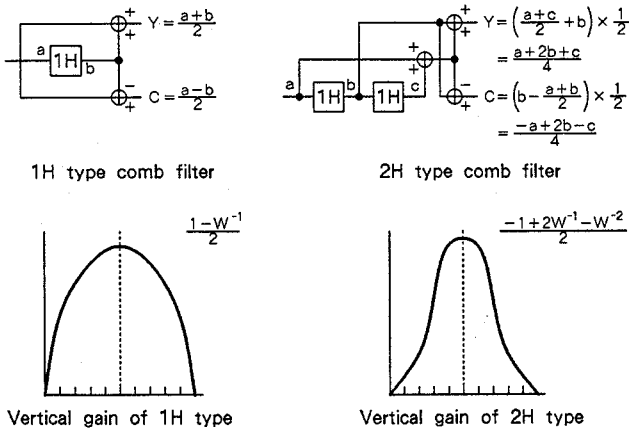


Fig. 10-9

As no correlation of C between lines is obtained with a Y/C separation circuit using a comb filter, C may leak to Y and 3.58MHz components of C may appear in dots. This is called "dot interference", which will be clearly observed on the borders between the EIA color bars and black-and-white portions and on the frames of superimposed pictures where colors change in the vertical direction.

To reduce the dot interference of the PD5087, a detection signal is generated by observing whether 3.58MHz components are found in the Y signal or not and checking the correlation of C between lines after separating Y and C with the comb filter. When the detection signal is generated, a trap is inserted in the Y signal separated with the comb filter to remove the 3.58 components. In other words, when there are no middle- or high-range components (regardless of the adjacency to 3.54MHz) and the chroma has a certain level which varies for 1H before and after, the trap is turned ON by judging the condition as dot interference.

Pin No.	Pin name	Function
3	DI00	Video input LSB ⋮ MSB
7	DI01	
9	DI02	
11	DI03	
14	DI04	
16	DI05	
18	DI06	
20	DI07	
2	DI10	1H/2H delayed video input LSB ⋮ MSB
5	DI11	
8	DI12	
10	DI13	
12	DI14	
15	DI15	
17	DI16	
19	DI17	
35	DO00	Y output LSB ⋮ MSB
30	DO01	
29	DO02	
28	DO03	
27	DO04	
26	DO05	
25	DO06	
24	DO07	
46	DO10	C output LSB ⋮ MSB
44	DO11	
43	DO12	
42	DO13	
40	DO14	
39	DO15	
38	DO16	
37	DO17	
55	DO2	Notch display pulse output.
80	CKI	CK (4fsc) input
79	DLIN	Delay CK (4fsc) input. When possible the internal delay cell is used. H or L
36	CKO	CK (4fsc) pulse
21	CKB	CK (8fsc) pulse
75	BPI	Blanking pulse input.

Pin No.	Pin name	Function
71	BPO	Blanking pulse output.
57	CHG	Internal/External switching of the delay CK. L : Use the internal delay cell. H : Use the DLIN input signal.
70	CI	Chroma inversion control. L : OFF H : ON (Inversion)
76	TOFF	Adaptive notch control.
77	TON	Notch ever on control. TOFF TON X H : Notch ever ON H L : Adaptive notch L L : Notch OFF
78	DTON	Detail notch control. L : OFF H : ON
67	SOL	Solarization control. L : OFF H : ON
69	A	Solarization level control. A B L L : MSB. MSB − 1 H L : MSB. MSB − 1. MSB − 2 L H : MSB. MSB − 1. MSB − 3 H H : MSB. MSB − 2. MSB − 3
68	B	
66	STB	Strobe signal (negative) input.
1	ET5	Detection levle control of the middle and high-pass gain elements of the Y signal. ET5 (MSB) ET4 ET3 4bit × 16 ET2 (LSB)
4	ET4	
6	ET3	
45	ET2	
48	YL1	Detection level control of the chroma. YL1 (MSB) YL0 ET1 4bit × 16 ET0 (LSB)
47	YL0	
41	ET1	
34	ET0	
54	SL1	Detection level control of the chroma correlation. SL1 (MSB) SL0 CL1 4bit × 16 CL0 (LSB)
53	SL0	
50	CL1	
49	CL0	
60	SEL	Control of pins 80 and 64. Pin 80 of IC : L (Fixed)
63	TP2	Test signal input At the IC is used : L (Fixed)
56	TP1	
51	TP0	
58	TM1	Test mode control At the IC is used : L (Fixed)
59	TM2	
60	TM3	

Table 10-1 Pin functions of PD5087

(4) PDB009 (Digital CNR)

A block diagram of PDB009 (digital CNR) is shown in Fig. 10-10.

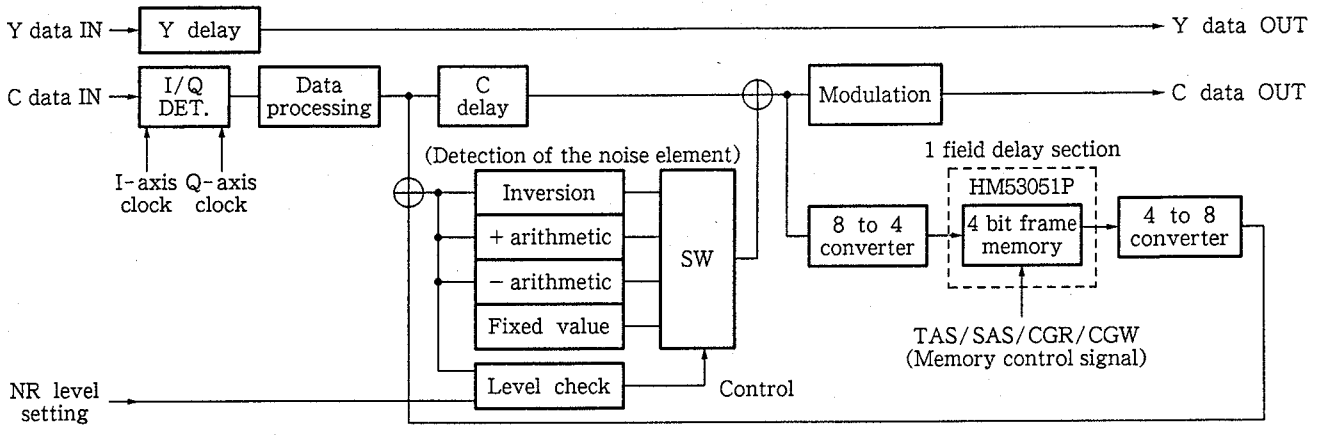


Fig. 10-10 Block diagram of the digital CNR (PDB009)

Pin No.	Pin name	Function	Pin No.	Pin name	Function
76	BI0	Video Y input (LSB ⋮ MSB)	57	CG R	D-RAM read timing output
77	BI1		36	BO0	Video Y output (LSB ⋮ MSB)
78	BI2		35	BO1	
79	BI3		34	BO2	
80	BI4		32	BO3	
81	BI5		30	BO4	
82	BI6		29	BO5	
83	BI7		28	BO6	
65	CI0	Video C input (LSB ⋮ MSB)	27	BO7	
66	CI1		26	DO0	Delayed video Y output (LSB ⋮ MSB)
67	CI2		25	DO1	
68	CI3		24	DO2	
69	CI4		23	DO3	
70	CI5		20	DO4	
71	CI6		19	DO5	
72	CI7		18	DO6	
74	CKO	Clock input for latch the Y.C.	17	DO7	
8	RDCK3	Clock input (4fsc)	47	CO0	Video C output (LSB ⋮ MSB)
2	HBL RTN	H-BLK input	46	CO1	
3	HBLR	H-BLK input	45	CO2	
4	R358	3.58MHz (fsc) input	44	CO3	
6	RV	Field timing input	41	CO4	
7	NR HBLO	Delayed H-BLK output	40	CO5	
60	WD0	D-RAM write data output (LSB ⋮ MSB)	39	CO6	
62	WD1		38	CO7	
61	WD2		37	BCKO	Clock output for Y. C.
59	WD3		16	DLKO	Clock output for delayed Y.
51	RD0	D-RAM read data input (LSB ⋮ MSB)	9	LS0	LSB ⋮ MSB: Setting input of NR level. Eight stages of 0 through 7.
49	RD1		11	LS1	
48	RD2		13	LS2	
50	RD3		15	ON	NR ON/$\overline{\text{OFF}}$
56	DRAMCK	D-RAM CLK output	14	FASA	ON/$\overline{\text{OFF}}$ input of the STILL picture NR.
55	SAS TAS	D-RAM reset output	5	CRM INV	Control input of the chroma inversion. L : OFF, H : ON
58	CG W	D-RAM write timing output			

Table 10-2 Pin functions of PDB009

(5) On pseudo 9-bit blocks of the LD-S2

When a signal B shifted in the direction of time by half a cycle is added to the original signal A having a bit resolution a (which corresponds with the D/A converter output) in the direction of level, the rates both in the level and time base directions will be halved. This increases the data before the D/A converter seemingly by 1 bit in the direction of level.

Also in the direction of time, the clock is seemingly doubled, providing an effect similar to that of the digital filter for a CD.

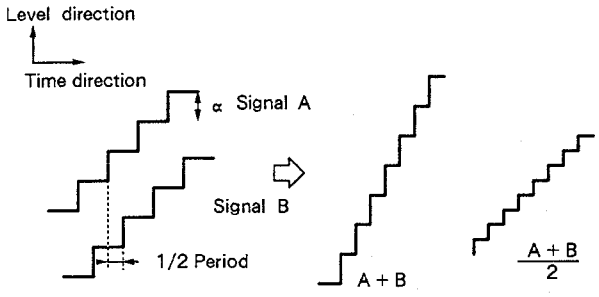


Fig. 10-11

(6) Composite sync insertion

Sync information is inserted into Y/C separated video data at IC23 (TC74HC4053AP). The phases of C sync and video signal must be matched in this stage.

As the video signal is delayed in processing at IC13 and IC18, the LD-S2 inhibits the 14-MHz master clock (IC15, IC16 and IC17) from being supplied to the PDB006 until the phase matches that of sync to be inserted by making the HBL which indicates the sync phase of the H address counter of the PDB006 pass through the same ICs.

Actually, without directly supplying the SG output to IC4, the sync after passing IC11 (PDB006) logic is inserted.

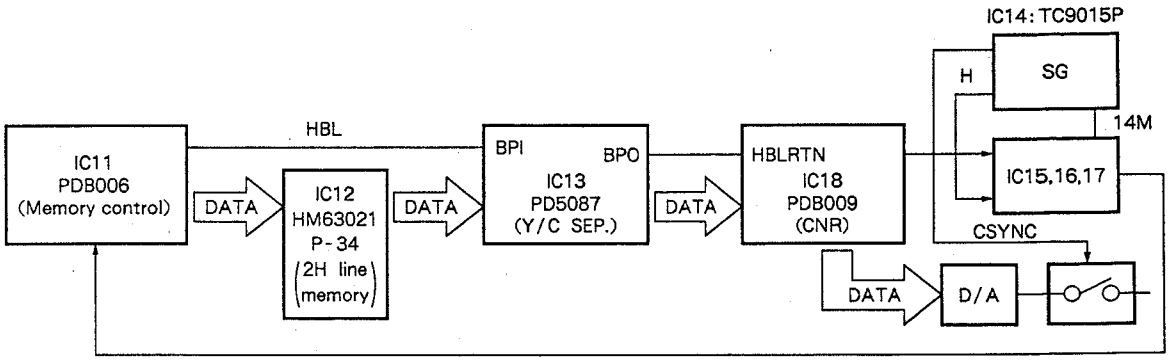


Fig. 10-12 Conceptional diagram of composite sync insertion

10.4 Digital Time Base Corrector

10.4.1 Overview

The configuration of a digital time base corrector (hereafter referred to as a digital TBC) is illustrated in Fig. 10-13.

In an analog TBC, a video signal containing a time base error (jitter) is transmitted to the CCD delay element in sequence to cancel the error by changing the clock and varying the transmission speed depending on the error.

In this way, the analog delay element absorbs time base errors by changing the delay time. However, some degradation cannot be eliminated including a change in the frequency response of video signals caused by the clock frequency which determines the delay time. With video signals which contain a large time base error, especially the color signals may be affected, generating flicker (picture shaking) on some screens. Therefore, the LD-S2 has employed the digital system which is superior to the analog system in time base error absorption.

For the delay element to absorb time base errors, a 1H line memory for digital data is used.

Digital data which contains an A/D (analog-to-digital) converted time base error is written in the 1H line memory by the clock which has the same time base error. By using a stable clock having a fixed frequency when reading, the time base error is absorbed in the 1H line memory.

When using digital data to absorb time base errors in this way, stable video signal output can be obtained with no signal degradation in the delay element stage. With analog systems, the delay element lies in the TBC servo loop, causing a small delay in the phase and providing only a little allowance. This disturbs the complete and faithful compensation for unevenness in colors.

On the contrary, the digital TBC has no delay element in the TBC loop, providing a large allowance, with which residual jitter can be reduced much more, and pictures with very little unevenness of colors can be obtained.

The PDB005 mainly performs VCO control to generate the write clock. The PDB006 performs VCXO control for the clock to read from field memory and spindle error generation.

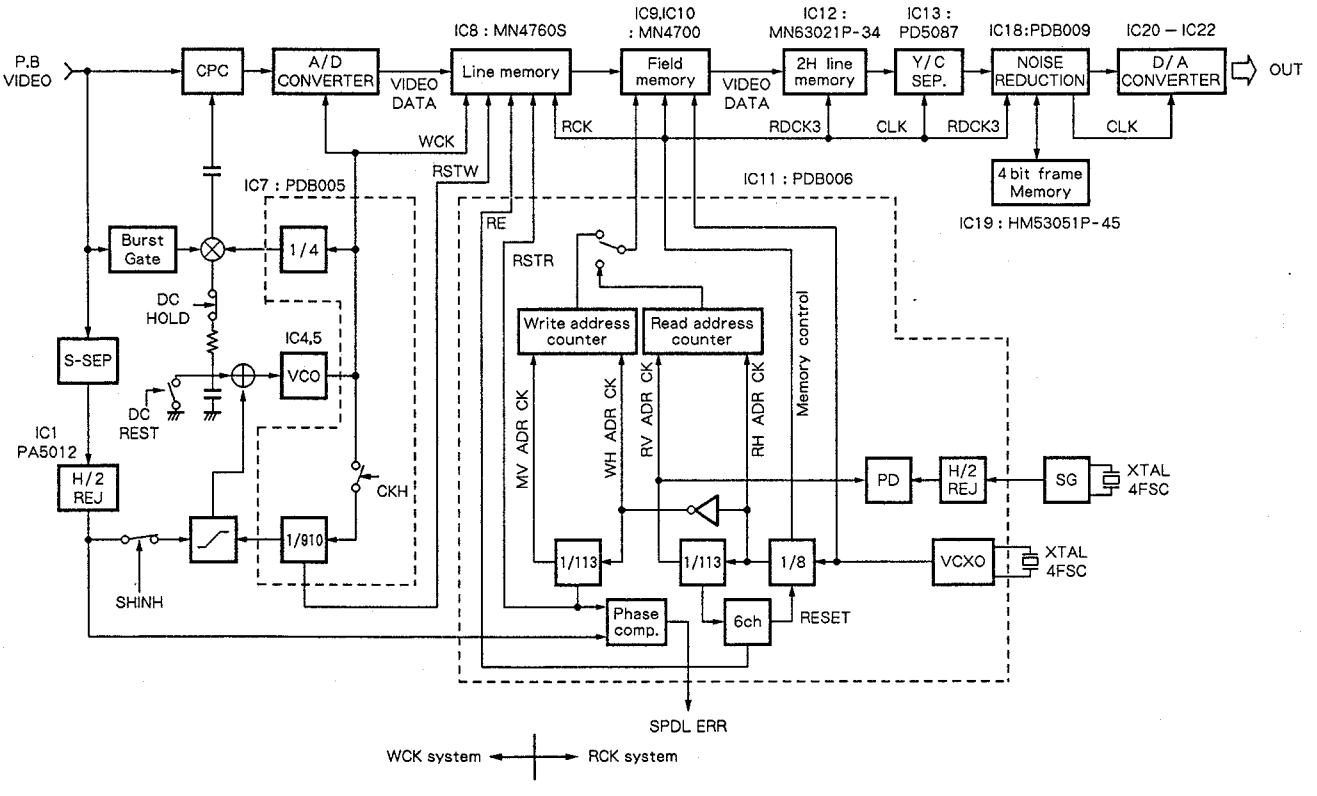


Fig. 10-13 Configuration diagram of the digital TBC (VSMB assembly)

10.4.2 On the digital TBC

Functions and relation to the SPDL servo of line memory

Line memory is also called FIFO (First In/First Out), which requires no address input, unlike normal memory ICs. Data will be read in the sequence in which they have been written. The respective address counters for write and read are provided inside the memory, for which the $\overline{WR}$ and $\overline{RD}$ signals are used as the reset signals for these counters respectively. And WCK and RCK function as the clocks for the respective counters.

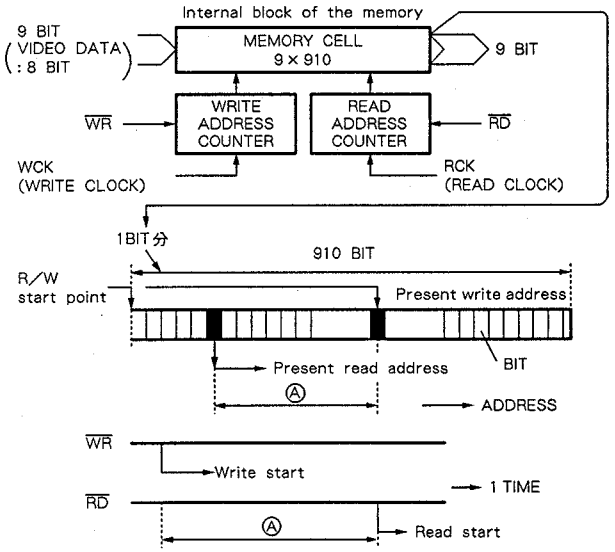


Fig. 10-14

When the $\overline{WR}$ signal becomes "L", the WRITE ADD. COUNTER is reset and increased in sequence, enabling data to be written to memory in sequence. When the $\overline{RD}$ signal subsequently becomes "L", the READ ADD. COUNTER is reset and increased in sequence and data are read in the sequence from that first written. Thus, as long as $\overline{WR}$ is ahead of $\overline{RD}$, the written data will be read after a delay of the period corresponding to the time lag between $\overline{WR}$ and $\overline{RD}$ (Fig. 10-14). The maximum delay time is determined by the capacity of the line memory. The capacity of the MN4760S is 910 samples, meaning that 910 addresses = 1H.

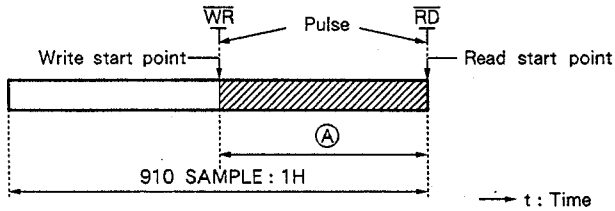


Fig. 10-15

Fig. 10-15 has been drawn by revising Fig. 10-14 to set the read start point to the right end. As A/D converted video signals are supplied to the line memory as data, both the $\overline{WR}$ and $\overline{RD}$ signals become "L" every 910 samples or every 1H. The $\overline{RD}$ signal here is generated by dividing the VCXO of 4 fsc into 910, the frequency of $\overline{RD}$ is stable, fixing read operations. In addition, if the $\overline{WR}$ signal is locked to the PBH, the period of Ⓐ in the Fig. 10-15 will change depending on the difference in frequency between $\overline{RD}$ and the PBH. If the frequency of the PBH is longer than that of $\overline{RD}$, the write timing is delayed compared to the read timing, the period of Ⓐ will become shorter and shorter and finally $\overline{WR}$ and $\overline{RD}$ align with each other, losing data to be read. Such a condition occurs when the SPDL rotation is slower than the proper rotation speed.

When the SPDL rotation is too fast, the frequency of the PBH or that of $\overline{WR}$ will shorten and become than that of $\overline{RD}$, expanding the period of Ⓐ, and data will finally overflow memory. Therefore, when the SPDL rotation is controlled to fix the period of Ⓐ, data will not overflow or underflow memory. For this, the conventional SPDL servo function can be used to lock the PBH to $\overline{RD}$. However, as the eccentric and jitter components cannot be absorbed only by the SPDL servo, the write start point or the position of $\overline{WR}$ may shift to the left or right.

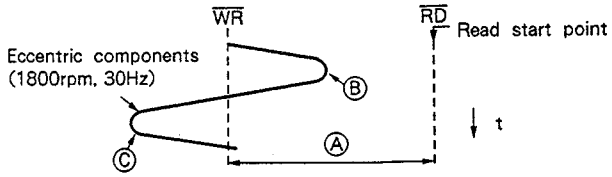


Fig. 10-16

Even if the position of a $\overline{WR}$ shifts to the left and right as shown in Fig. 10-16, data can be read without any overflow or lack as long as the eccentric components do not exceed Ⓐ. In other words, the line memory functions as a variable delay line in the same manner as a conventional CCD and absorbs the eccentric component. The difference from a CCD is that the signal degradation caused by changes in the conventional CCD clock is eliminated in digital processing using A/D converted data.

Actually, the SPDL servo operates so that Ⓐ in Fig. 10-16 will become about H/2, permitting eccentric components of about $\pm 30\mu S$ to be absorbed in the line memory for an appropriate time base compensation.

Timing of A/D conversion

At point Ⓑ in Fig. 10-17, the frequency of the PBH is longer than that of REF H and consequently the period of 1H becomes longer than usual, which becomes on the contrary shorter than usual at point Ⓒ. (See Fig. 10-17.) Even when the length of 1H changes, the number of samples for A/D conversion must be fixed to 910. Therefore, the frequency of the A/D conversion clock must change according to eccentric components. This A/D conversion clock is also used as WCK or the clock for the address counter of line memory.

As the VPS processing is also executed for video signals before A/D conversion, REFSC for VPS error detection must also change according to the eccentric components. Therefore, the A/D conversion clock is divided by 4 and used for comparison with the burst to detect VPS errors.

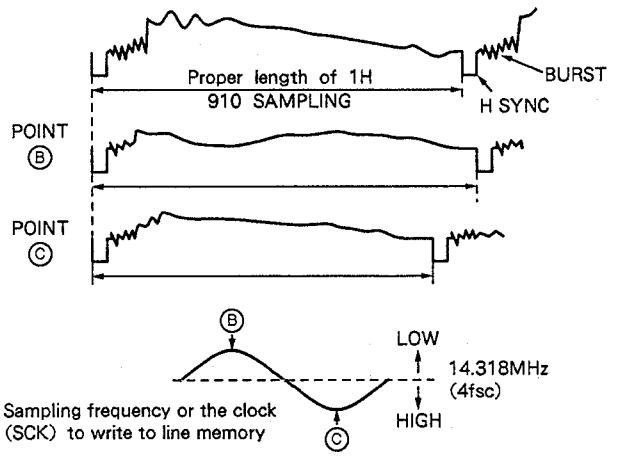


Fig. 10-17

10.4.3 Operations of the PDB005

Write clock generation

To generate the clock which changes according to eccentric components, the PDB005 and the PA5012 provide a loop to control the 910fH VCO. (See Fig. 10-13.) The output of the 910fH VCO is supplied to pin 10 of the PDB005 and output as REF H from pin 21 after being divided into 910. This REF H output is supplied to pin 7 of the PA5012. A trapezoidal signal for error detection rises up synchronizing with the falling edge of REF H, and a sample-and-hold operation is executed at the falling edge of the PBH supplied from pin 1, detecting errors in the H rate. (See Fig. 10-18)

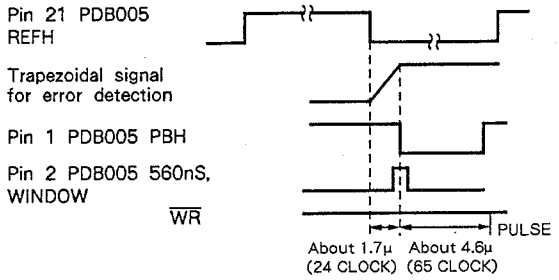


Fig. 10-18

VCO loop control

To detect the lock condition of the 910fH VCO loop composed of the PA5012 and the PDB005, the falling edge of the PBH is checked inside the PDB005 to determine whether it is in a pulse of 560 nS width for locational detection. This pulse of 560 nS is obtained by dividing the VCO output, and the rising edge of the pulse is positioned about 1.4μ (corresponds with 20 clocks) apart from the falling edge of REF H. This pulse for detection is once output from pin 2 of the PDB005 and immediately supplied to the DC RESET DET block from pin 1.

As shown in the figure below, the pulse for detection is latched at the falling edge of the PBH in the DC RESET DET block. If the position of the PBH shifts, the latch output will become "L".

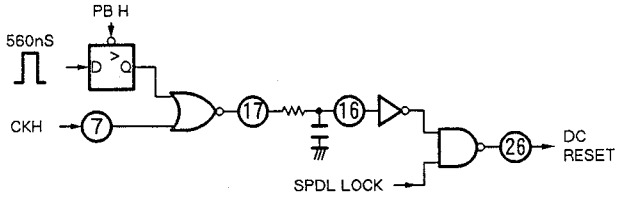


Fig. 10-19

When the latch output becomes "L", pin 17 changes from "L" to "H" and DC RESET at pin 26 becomes "H" subsequent to the time constants at pin 16 and pin 17. This sets the SW at pin 30 in the PA5012 to ON, resetting burst errors to 0. Consequently, the VCO loop is controlled only by the H error, positioning the falling edge of the PBH in the center of the 560 nS pulse. (This is because the inclination of the trapezoidal signal for H error detection was adjusted so that the PBH is positioned in the center of the 560 nS pulse when the burst error is 0.)

When the SPDL servo is not locked or during a reference shift operation (when CKH at pin 7 is "H"), the DC RESET becomes "H", resetting the burst error detection block.

The DC HOLD signal is also supplied from pin 43 of the PDB006 to the burst error detection block of the PA5012 in the following cases so that the position to start writing to line memory (or the phase of $\overline{WR}$) is not shifted once fixed.

1. When CKH is "H".
2. When the relation between the phases of $\overline{WR}$ and $\overline{RD}$ for line memory is drastically disturbed.

The $\overline{S/H\ INH}$ signal which inhibits error S/H as required is supplied also to the H error detection block of the PA5012 from pin 22 of the PDB005. While CKH supplied to pin 7 of the PDB005 is "H" or during a reference shift operation, REF H is held as with conventional systems and the S/H INH also becomes "L", eliminating the H error S/H. The $\overline{S/H\ INH}$ becomes "L" also when the SPDL is not locked. When any drop out is detected in the period between the start of the trapezoidal signal for H error detection and the falling edge of the PBH, the $\overline{S/H\ INH}$ signal will become "L" as any error S/H is not performed by the original PBH.

	When SPDL is UNLOCK	CKH = H
$\overline{S/H\ INH}$	L (ON)	L
DC HOLD	L	H (ON)
DC RESET	H (ON)	L

Table. 10-3

Functions of other blocks in the PDB005

< CHROMA DET block >

This block extracts PB burst signals from the PB burst from pin 32 and the BF (burst flag) from pin 31 and detects the burst phase of every 1H by comparing the burst signals with those obtained by dividing the VCO output by 4. The REF SC to be sent to the PA5012 is reversed so that it has a fixed relation to the detected PB burst phase. The result of the PB burst phase detection is output from pin 3 as the PCR (Play Chroma) signal, which is supplied to pin 50 of the PDB006.

< WV and WF signal generation >

WV: Obtained by latching the PBV signal supplied from pin 35 using $\overline{WR}$.
This signal will be supplied to pin 48 of the PDB006 and start vertical addressing of field memory.

WF: Obtained by latching REF H using the PBV.
This signal indicates whether the video data written to the field memory is the first field or the second field, which is supplied to pin 49 of the PDB006.
The PDB006 reads data from the field memory in synchronization with the C-SYNC supplied from the sync generator, which is not synchronous with the write SYNC signal (PB-V, PBH).
Therefore, it is necessary to previously know whether the data is the first or the second field when reading it from field memory. The WF signal is used for this purpose.

10.4.4 Functions and operations of the PDB006

Data reading from line memory and control of video memory

The video data read from the line memory is divided into upper 4 bits and lower 4 bits and immediately written in video memory (MN4700). The timing ($\overline{RD}$ signal) of reading from line memory must be synchro-nous with the timing of writing to video memory. The timing of writing in the video memory or the RAM write address is generated by the WRITE ADDRESS GEN. in the PDB006 and, therefore, the $\overline{RD}$ signal for line memory is also generated in the same block. Fig. 10-20 depicts data for one field to be written to video memory.

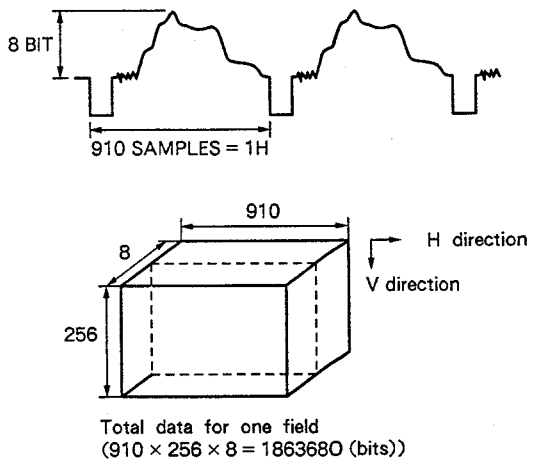


Fig. 10-20

The LD-S2 can store a 1-field picture by using a pair of 1Mbit DRAMs (MN4700). An 8-bit data item is divided into upper 4 bits and lower 4 bits and written to these two DRAMs. As the vertical addresses of DRAM number $256 = 2^8$, a part of the V-SYNC is not written to memory in the same manner as conventional with LD players equipped with video memory.

The MN4700 is equipped with an 8-bit shift register for a single data bus and processes the input data only 8 bits at a time. Consequently, 6 samples remain when dividing 910 samples available in the horizontal direction by 8 (910/8 = 113 with 6 left over). Therefore, by specifying horizontal addresses to 0 through 112 so that the address counter stops operating for the 6 remaining samples, they are eliminated from being written to memory. (See Fig. 10-21.)

The DRAM write addresses are generated at the WRITE ADDRESS GEN. block in the PDB006. As the start of addressing is triggered by the WV signal supplied to pin 48 of the PDB006 from pin 5 of the PDB005, writing to DRAM synchronizes with the PBV. The DRAM read addresses are generated in the READ ADDRESS GEN. block and triggered by the REF C -SYNC signal supplied to pin 99 of the PDB006 from the SYNC GEN. IC.

The clocks of these two ADDRESS GEN. are obtained by dividing the 4fsc or 910fH clock by 8 and line memory read clock is the original 910 fH clock before the frequency division. This means that all operations after that to read from the line memory are controlled by the same clock.

This is because the PDB006 uses the 910 fH clock for all its operations.

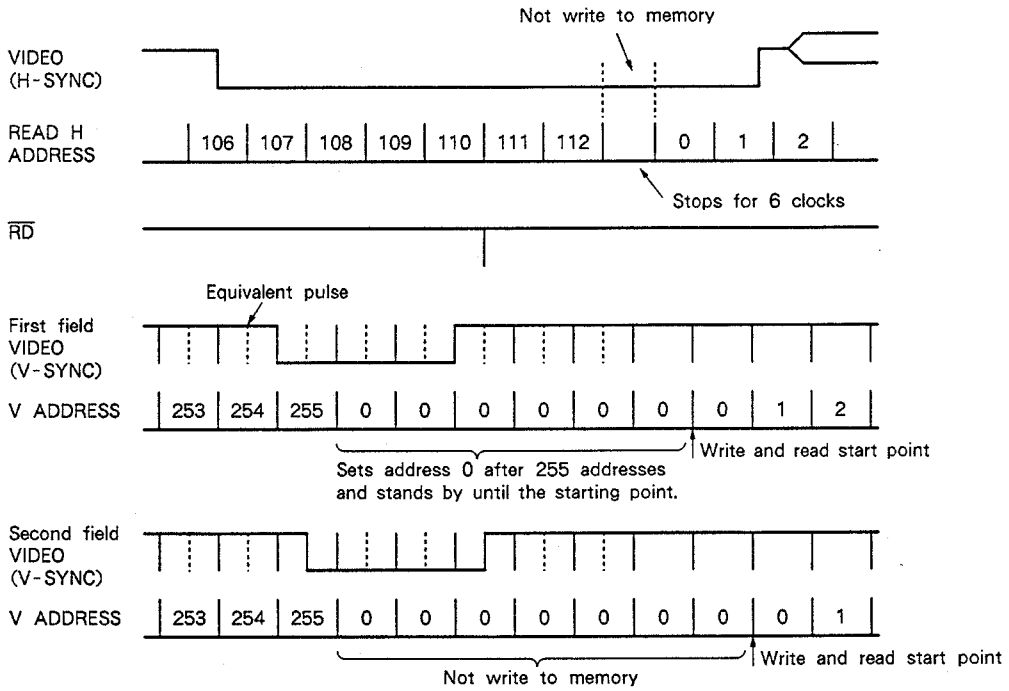


Fig. 10-21 Relation of H and V addresses to the actual video signals

910fH VCXO control by the PDB006

The PDB006 operates by using the 910fH VCXO output which is synchronous with the REF C-SYNC supplied to pin 99 from the SYNC GEN. IC VSMB assembly of IC14 (TC9015P) as the master clock.

Chroma determination and 140 nS shift operation in the PDB006

The PCR signal supplied to pin 50 of the PDB006 is written to field memory by being inserted in the LSB of the video data at horizontal write address 1 of field memory.

This data is used to judge the continuity of the chroma (burst) phase when being read from field memory. The result of the judgement of being continuous or discontinuous is supplied from pin 102 as the CRM INV signal directly to pin 103. The delay of 140 nS to maintain the continuity of the burst is handled by delaying the video data to be output to the D/A converter by 2 clocks (= 140 nS).

As the C-SYNC signal output from pin 100 is delayed for 140 nS by the time constant connected between pin 104 and pin 105, the SYNC is also delayed when the video data is delayed for 140 nS.

Operations of the SPDL SERVO CONT block

When a reference shift operation is executed during a CLV scanning or jump operation, data writing to video memory is held. The CKH at pin 46 of the PDB006 then becomes "H" and the VCO loop control for writing to line memory is executed in the PDB005. Simultaneously, the RFST at pin 45 of the PDB005 becomes "H", notifying the main CPU that a reference shift operation has been executed. At the same time, the SPDL REF is also shifted. The main CPU outputs to execute a reference shift and the SPDL servo operates to align the edge of the SPDL REF to that of the PBH.

The SPDL servo controls the disc rotation or the $\overline{WR}$ frequency so that the lag between $\overline{RD}$ and $\overline{WR}$ is always kept to about 30μS. However, excessive eccentration or a scanning operation may disturb the relation between $\overline{RD}$ and $\overline{WR}$, disabling the reading of data from line memory. Therefore, the positions of the pulses corresponding to horizontal addresses 98 through 105 and 102 through 105 and the rising of the PBH are checked as shown in Fig. 10-22 to observe the positions of $\overline{RD}$ and $\overline{WR}$.

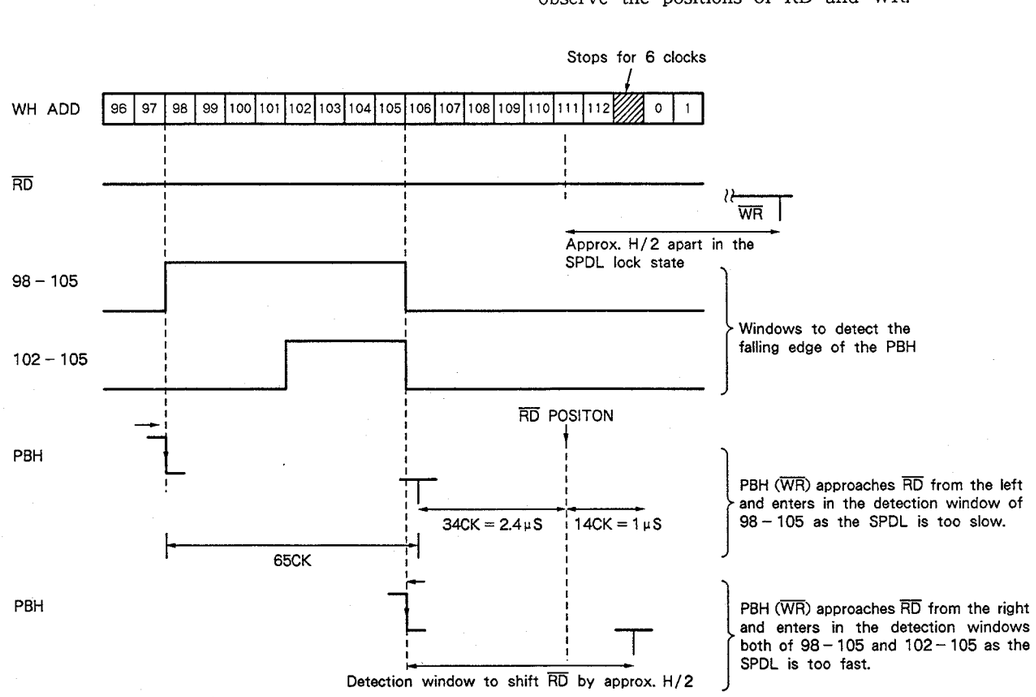


Fig. 10-22 Timing and detection when the SPDL is too slow or too fast

The operations when SPDL rotation is slower or faster than the proper speed are described below.

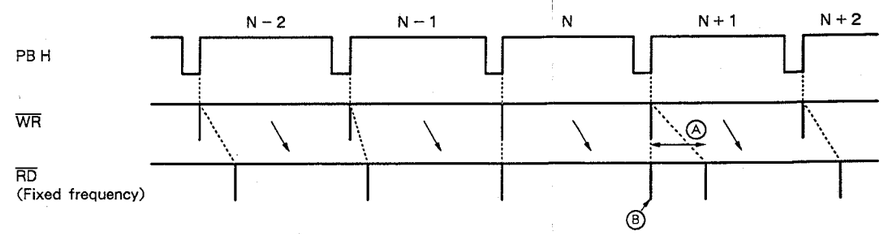


Fig. 10-23 When SPDL is slow

In this case, as the frequency of $\overline{WR}$ is longer than that of $\overline{RD}$, $\overline{WR}$ approaches $\overline{RD}$ from the left. If no measures are taken, $\overline{RD}$ will finally catch up with $\overline{WR}$ and the data on that line will be read twice. To avoid this, 56 is loaded as the initial value of the next H address counter (which counts from 0 to 112) when detecting that the PBH falling edge enters in the detection window of 98–105. Thus, the next $\overline{RD}$ (which corresponds to the position at H address 111) will be positioned H/2 (the period of Ⓐ in Fig. 10-23) apart from $\overline{WR}$.

Consequently, the data on line (N+1) is read at $\overline{RD}$ on point Ⓑ and read again from the beginning at the next $\overline{RD}$ which is delayed for the period of Ⓐ from point Ⓑ. Thus, the proper locational relation between $\overline{WR}$ and $\overline{RD}$ has been resumed by shifting $\overline{RD}$ by H/2. As writing to line memory is always continuously performed, no data is lost and the picture is not affected even when $\overline{RD}$ is shifted by H/2. As data read from line memory is written in field memory, writing to field memory is inhibited during the period of Ⓐ in Fig. 10-23.

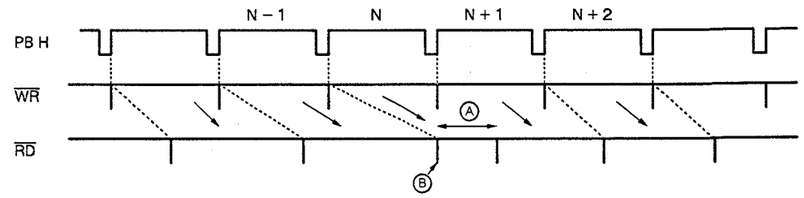
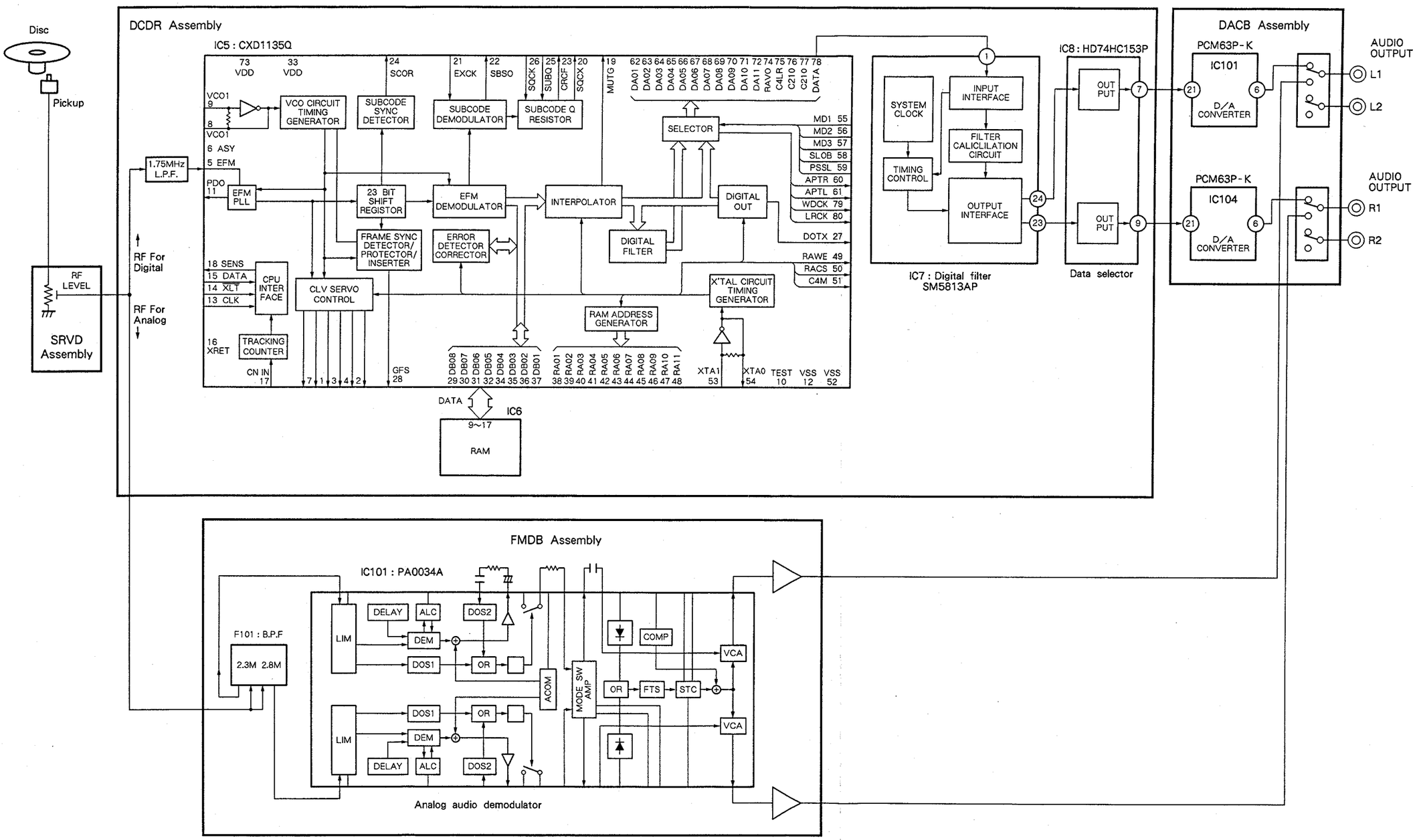


Fig. 10-24 When SPDL is fast

In this case, as the frequency of $\overline{WR}$ is shorter than that of $\overline{RD}$, $\overline{WR}$ approaches $\overline{RD}$ from the right. If no measures are taken, $\overline{WR}$ will finally catch up with $\overline{RD}$ and some data on that line may not be read. $\overline{WR}$ approaching $\overline{RD}$ from the right means that the falling edge of the PBH approaches the detection pulses of 98–105 and 102–105. When the PBH falling edge enters in these two detection pulses, 56 is loaded as the initial value of the horizontal address counter, shifting $\overline{RD}$ by the period of Ⓐ. However, unlike the case where "SPDL is slow", data on line (N+1) is read when reading data at $\overline{RD}$ delayed for the period of Ⓐ. Consequently, data on line N is not read from line memory and data for 1H to be written in field memory is lost.

The lost data for 1H is compensated for by subtracting 2 from the vertical address and replacing it with the data 2H before when reading from field memory. To indicate that $\overline{RD}$ has been shifted by H/2, the LSB of the H address (at the head) on line N+1 is set to "1" and written to field memory, which is called "SHIFT DATA".

10.5 AUDIO CIRCUIT DESCRIPTION



10.5.1 RF signal route

The RF signals containing audio components from the SRVD assembly are divided at the DCDR assembly and those for analog audio are processed at the FMDB assembly and those for digital audio are processed at the DCDR assembly.

Analog audio signal processing

The RF signals for analog audio sent to the FMDB assembly enter a B.P.F. (band-pass filter) of F101, divided into two audio FM signals of 2.3 MHz (channel L) and 2.8 MHz (channel R) and sent to IC101 (PA0034A).

At IC101 (PA0034A), the following processing opera -tions are performed, outputting analog audio signals.

- FM demodulation
- Previous value hold
- De-emphasis
- VCA (Voltage-controlled amplification)

Pin	Pin name	Function	Pin	Pin name	Function
1	VEER	Power supply	22	LOUT	L ch output
2	VINR	FM signal input	23	STC2	STC pin 2
3	BIASR	Input bias	24	STC1	STC pin 1
4	VREFR	Internal reference power supply	25	VCC	Power supply
5	GNDR	GND	26	COMP	Compensator pin
6	ALCR	ALC capacitor pin	27	TBC	TBC error signal input
7	CSR	Carrier elimination	28	CINL	CX control signal input
8	DOS2R	DOS2 input	29	CXINL	CX input
9	DEMOR	Demodulation output	30	SWOL	Amplifier output of the mode switch
10	SINR	Switch input of the drop out correction	31	SWINL	Amplifier input of the mode switch
11	DOCR	Switch output of the drop out correction	32	DOCL	Switch output of the drop out correction
12	SWINR	Amplifier input of the mode switch	33	SINL	Swtich input of the drop out correction
13	SWOR	Amplifier output of the mode switch	34	DEMOL	Demodulation output
14	CXINR	CX input	35	DOS2L	DOS2 input
15	CINR	CX control signal input	36	CSL	Carrier elimination
16	R	Mode switch R	37	ALCL	ALC capacitor pin
17	L	Mode switch L	38	GNDL	GND
18	CX	CX control	39	VREFL	Internal reference power supply
19	FTC	Connect a capacitor for FTC	40	BIASL	Input bias
20	GNDCX	GND	41	VINL	FM signal input
21	ROUT	R ch output	42	VEEL	Power supply

Table. 10-4

Digital audio signal processing

The FM signals containing digital audio components are sent to an L.P.F. (low-pass filter) of 1.75 MHz via an amplifier composed of the DCDR assembly IC1 (TC40H004P) and then sent to IC5 (CXD1135Q) as EFM signals.

The CXD1135Q has the following functions.

1. Reproduction of the bit clock (PLCK : 4.3218 MHz) by the EFM PLL
2. EFM signal demodulation, error correction and interpolation
3. Detection, protection and insertion of frame sync signals
4. Sub-code signal demodulation and error detection
5. SPDL servo (forced acceleration, braking, speed servo, phase servo)
6. Zero cross counter for 8-bit tracking errors
7. Two-pass oversampling digital filter (35th order)
8. Digital audio interface output

The internal block and terminal functions are shown in Fig. 10-25.

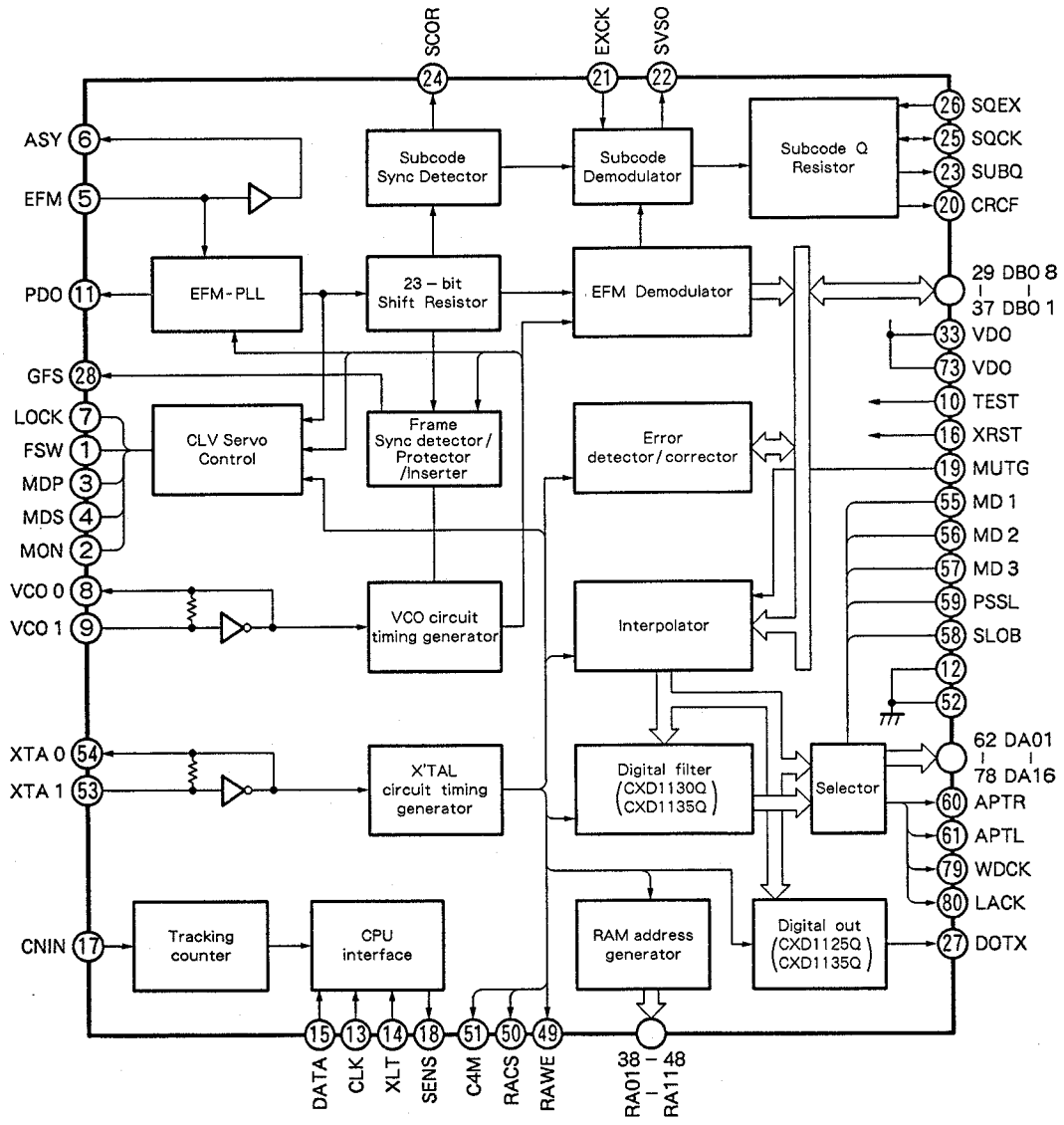


Fig. 10-25 Internal block diagram of CXD1135Q

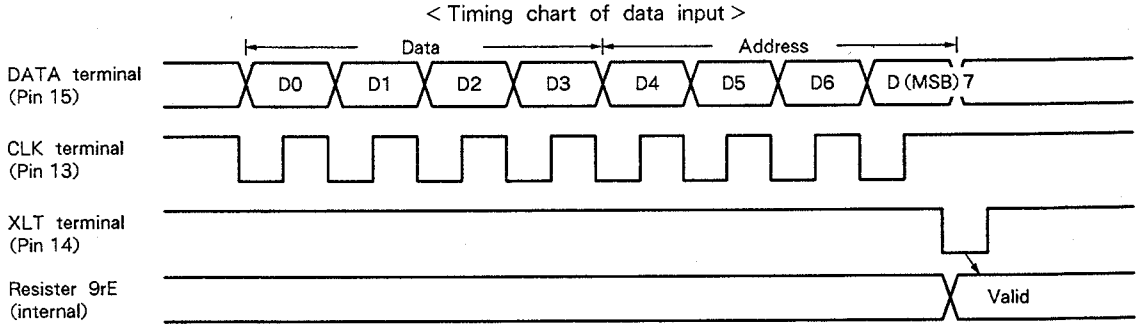
CXD1135Q command codes

The CXD1135Q has a 4-bit register having addresses from 9 through E as shown in the table below and can be operated by supplying command codes, each totaling of total 8 bits including address and data, to these registers.

Resister name	Command	Address D7 – D4	Data				Terminal (Pin 18)
			D3	D2	D1	D0	
9	New function control	1001	ZCMT	HZPD	NCLV	CRCQ	Z
A	Sync protection and attenuator control	1010	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set for lower 4 bits	1011	Tc3	Tc2	Tc1	Tc0	COMPLETE
C	Counter set for upper 4 bits	1100	Tc7	Tc6	Tc5	Tc4	COUNT
D	CLV control	1101	DIV	Tz	Tp	GAIN	Z
E	CLV mode	1110			CLV mode		Pw ≧ 64

The registers B and C are used as the zero cross counter for tracking errors.

Table 10-5



※ The supplied command is executed when the XLT terminal becomes "L" after an 8-bit data item is supplied.

Fig. 10-26

< Description of the registers >

● Register 9

ZCMT : Turns on and off the zero cross mute function.

HZPD : Turns on and off the function to set the PDO output (which controls the VCO by comparing the phases of the PLCK and the playback EFM) to Hi-Z for a period of max. 0.55 nsec. from the falling edge of the GFS (which becomes "H" when the SPDL locks).

NCLV : Selects the methods to detect SPDL phase servo errors when the PLL is locked.

CRCQ : Turns on and off the function to output CRCF information from the SUBQ terminal which outputs the subcode data Q.

After the bits of register 9 are all set to 0 by a power-on reset, no setting is performed for this register.

		Dn = 0	Dn = 1
ZCMT	D3	Zero cross MUTE off	Zero cross MUTE on
HZPD	D2	The PDO terminal is active.	The PDO terminal is set to Z at the GFS falling edge.
NCLV	D1	CLV-P servo by the frame sync signal	CLV-P servo by the base counter
CRCQ	D0	CRCF is not superimposed in SUBQ	SUBQ = CRCF at the SCOR rising edge

(The same functions as those of the CX23035) (New functions)

Table. 10-6

● Register A

This register controls four signals, GSEM, GSEL, WSEL and ATTM.

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

Table 10-7

With GSEM and GSEL, the register sets the number of times to interpolate a quasi frame sync when the frame sync is not correctly detected. It is set to 8 frames in all LD play modes and during CD playback and 13 frames in a scanning operation.

WSEL	Clock
0	±3
1	±7

Table 10-8

To prevent erroneous detection when detecting the frame sync, a detection window having a certain width is specified, ignoring sync patterns outside the window. With WSEL, the register sets the width of this window (to be set to ±7 clocks).

ATTM	MUTG terminal	dB
0	0	0
0	1	−∞
1	0	−12
1	1	−12

Table 10-9

MUTE ON/OFF and −12 dB attenuation are controlled in combination with the MUTG terminal (pin 19). $AA is supplied as the actual command code. As A = 1010 which means GSEM = 1 and GSEL = 0, the number of frame interpolation is set to 8 and the width of the detection window is set to ±7 clocks.

● Resister D

DIV	D3	0	RFCK/4 and WFCK/4	Phase comparison frequency at CLV-P mode
		1	RFCK/8 and WFCK/8	
TB	D2	0	RFCK/32	Bottom hold period at CLV-S and CLV-H modes
		1	RFCK/16	
TP	D1	0	RFCK/4	Peak hold period at CLV-S mode
		1	RFCK/2	
GAIN	D0	0	−12dB	Gain of MDP terminal at CLV-S and CLV-H mode
		1	0dB	

Table 10-10

RFCK : Read Frame Clock (7.35 kHz obtained by dividing the crystal oscillation)

WFCK : Write Frame Clock (Frame sync in playback EFM signals)

CLV-P mode : Phase servo which operates when the PLL loop is locked

CLV-S mode : Speed servo which operates when the PLL loop is not locked

CLV-H mode : Speed servo during search operations (or while the pickup is moving)

$D4 is supplied as the actual command code.

As 4 = 0100, it defines the phase error to the frequencies of RFCK/4 and WFCK/4, the bottom hold in CLV-S mode to the frequency of RFCK/16, the peak hold to the frequency of RFCK/4 and the gain at the MDP terminal to −12 dB.

When actually activating the SPDL, forced activation is executed in KICK mode by $E8 or 1000 after checking that the focus servo is locked, then CLV-A mode is set by $E6, closing the SPDL servo and PLL loop. Whether they are locked can be checked by observing whether the GFS becomes "H".

When stopping the SPDL, it is braked by $EA or 1010 and the stop mode is set by $10 after detecting at FG that the SPDL has stopped.

In addition, a toss link for optical fibers is connected as a digital output terminal to pin 27 via a buffer. Data output modulated in the digital audio interface format is obtained from pin 27 of the CXD1135Q. These digital filter and output functions can be activated and deactivated by setting MD1, 2 and 3 at pin 55, 56 and 57 to "L" or "H". With the LD-S2, digital filter OFF and digital output ON will be specified when MD1, 2 and 3 are set to "L", "L"and "H" respectively.

● Register E

Sets the operation modes of the SPDL servo. The SENS terminal or pin 19 becomes "L" when the pulse width of the frame sync detected in CLV-S mode is less than 64T. This register output is unused.

		(Pin 3)	(Pin 4)	(Pin 1)	(Pin 2)
Mode	D3−D0	MDP terminal	MDS terminal	FSW terminal	MON terminal
STOP	0000	L	Z	L	L
KICK	1000	H	Z	L	H
BRAKE	1010	L	Z	L	H
CLV-S	1110	CLV-S	Z	L	H
CLV-H	1100	CLV-H	Z	L	H
CLV-P	1111	CLV-P	CLV-P	Z	H
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	L or Z	H
CLV-A'	0101	CLV-S' or CLV-P	Z or CLV-P	L or Z	H

Table 10-11

Signal processing and peripheral circuits of the CXD1135Q

The EFM signal is amplified by the DCDR assembly IC1 amplifier and supplied to pin 5 of IC5 (CXD1135Q). The result of comparison between the EFM signal and the VCO output of IC3 (1/2) is output from pin 11 of IC5 to control the VCO, thus providing the PLL loop. The IC5 also detects SPDL servo errors from the EFM signal, whose pin 1 through 4 are used for the SPDL servo output.

Functions of the terminals are as follows.

FSW (pin 1): Hi-Z when the PLL loop is locked and L in other cases.
IC3 (1/2) (NJM082D) which functions as a mix filter both for phase and speed error is used to switch the cutoff frequencies. (Hi-Z : 500 Hz, L : 20 Hz)

MON (pin 2): L when the motor is stopped and H while it is rotating.

MDP (pin 3): SPDL phase error when the PLL is locked and speed error otherwise

MDS (pin 4): Speed error when the PLL is locked and Hi-Z in other cases

Whether the PLL is locked or not is internally detected. When the PLL is locked, the GFS terminal of pin 28 becomes "H".

Digital filter SM5813AP

The DCDR assembly of IC7 (SM5813AP) is an 8-times oversampling digital filter of the 18-bit output type. It executes 8-pass oversampling in the 3-stage connection of FIR 153 (rd) +29 (th) +17 (th) orders. A conceptual diagram of the oversampling is shown in Fig. 10-27.

D/A converter PCM63P-K

The DACB assembly of IC101 and IC104 (PCM63P-K) is a D/A converter of the resistance-ladder type which converts 18 bit-data from a digital filter into analog data, whose output represents current. This output is converted from current to voltage in the next stage of IC102 and 1C105 (NJM5534DD), setting the output voltage to 2.3 Vrms (0 dB).

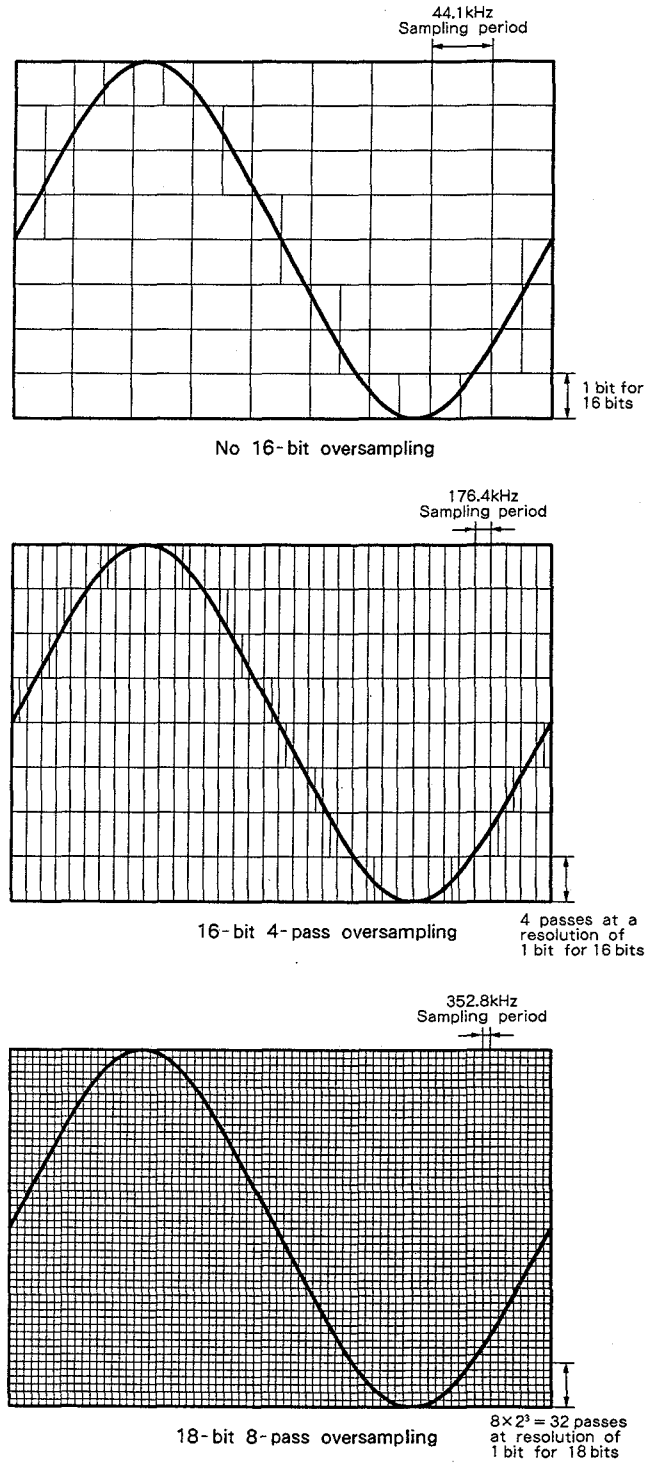
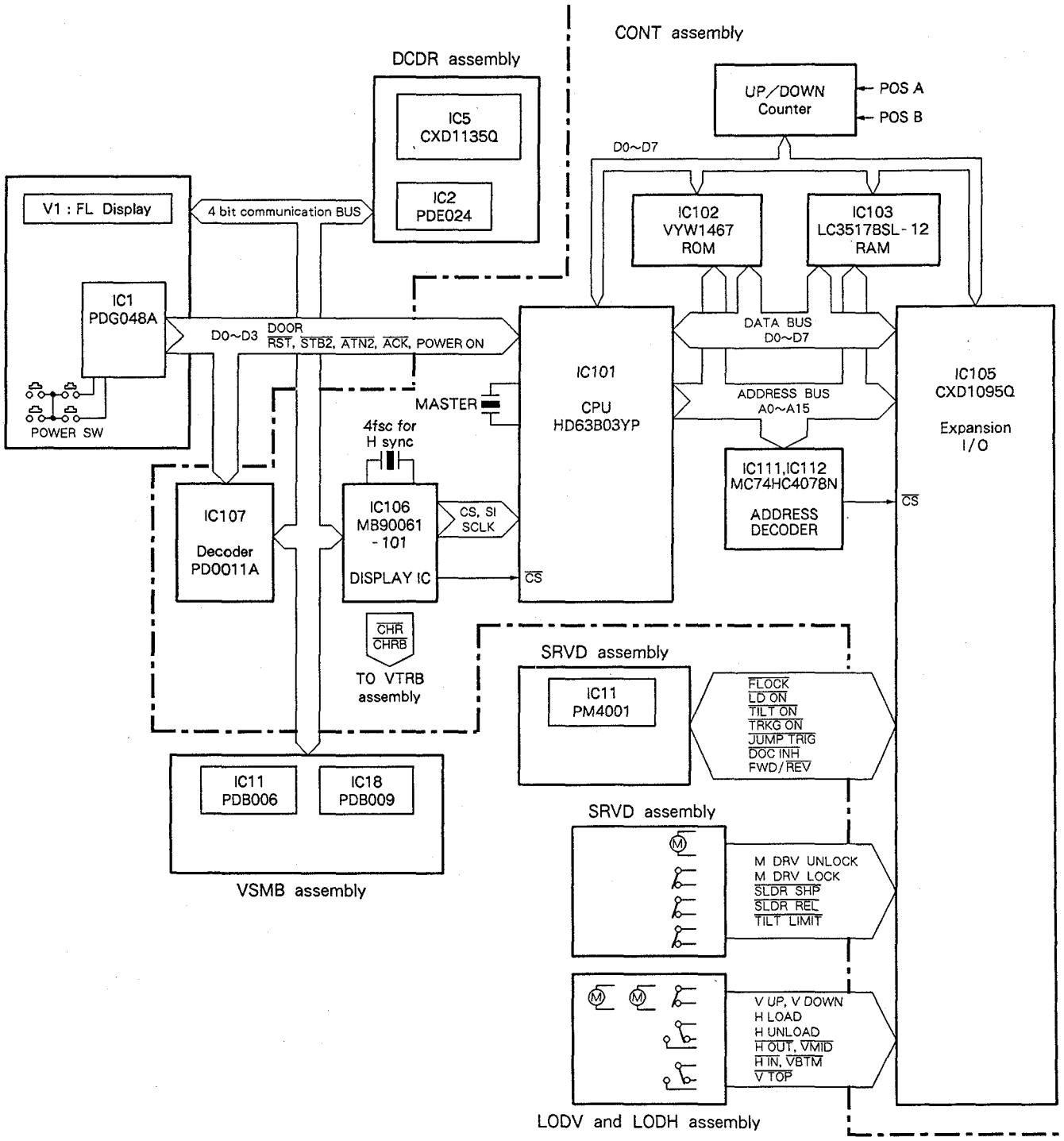
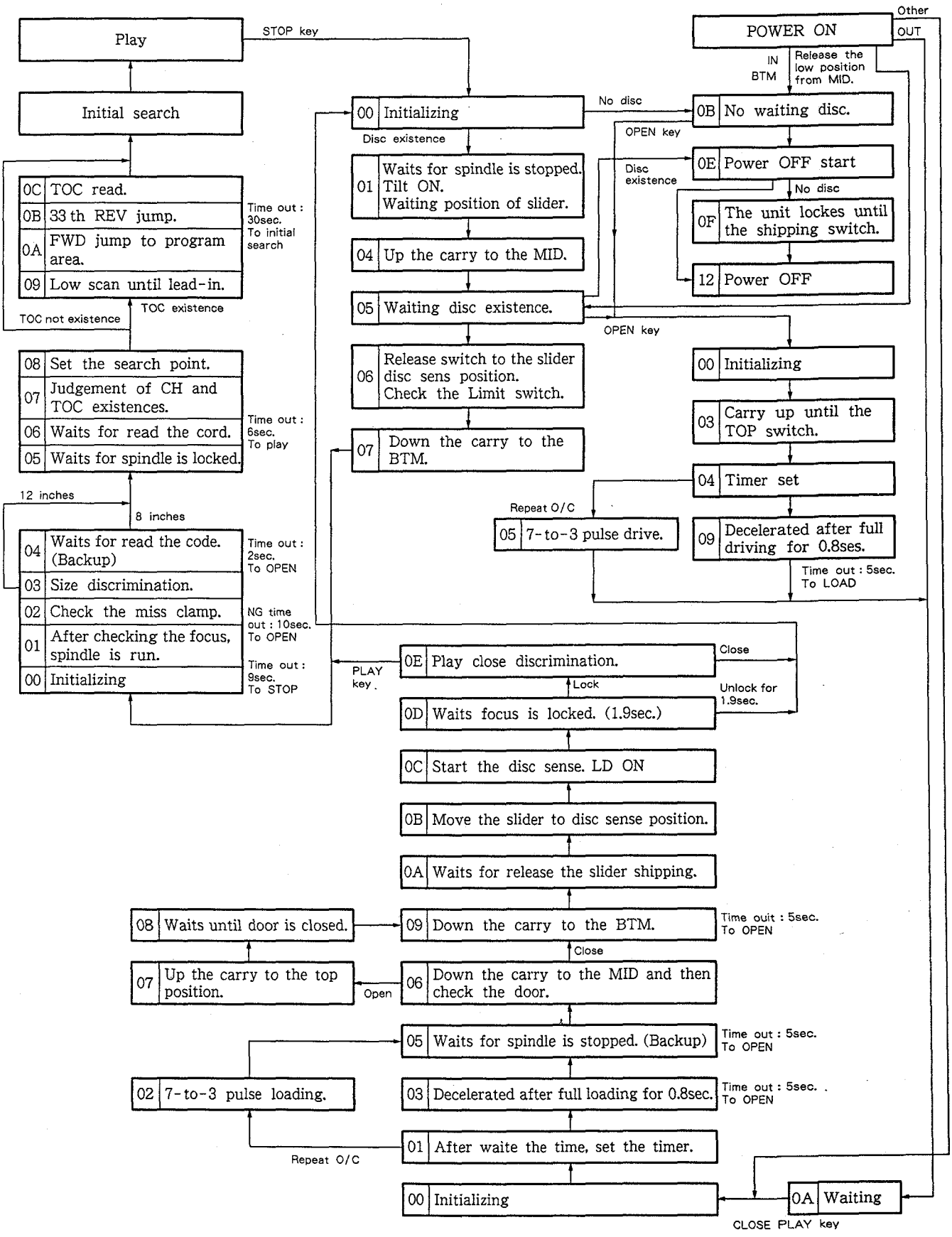


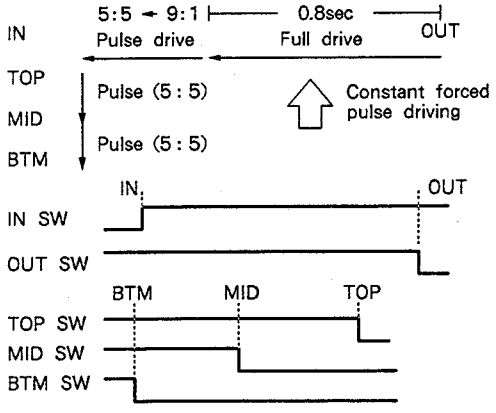
Fig. 10- 27 Conceptual diagram of the over sampling

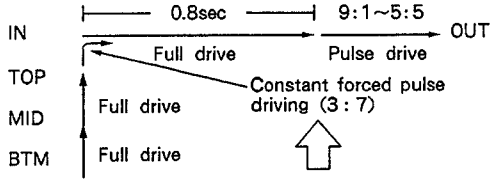
10.6 Software description of the microcomputer




Play
STOP key
Initial search
0C TOC read.
0B 33 th REV jump.
0A FWD jump to program area.
09 Low scan until lead-in.
Time out : 30sec. To initial search
TOC not existence
TOC existence
08 Set the search point.
07 Judgement of CH and TOC existences.
06 Waits for read the cord.
05 Waits for spindle is locked.
Time out : 6sec. To play
12 inches
8 inches
04 Waits for read the code. (Backup)
03 Size discrimination.
02 Check the miss clamp.
01 After checking the focus, spindle is run.
00 Initializing
Time out : 2sec. To OPEN
NG time out : 10sec. To OPEN
Time out : 9sec. To STOP
00 Initializing
Disc existence
01 Waits for spindle is stopped. Tilt ON. Waiting position of slider.
04 Up the carry to the MID.
05 Waiting disc existence.
06 Release switch to the slider disc sens position. Check the Limit switch.
07 Down the carry to the BTM.
No disc
OPEN key
POWER ON
Other
OUT
IN
BTM
Release the low position from MID.
0B No waiting disc.
0E Power OFF start
Disc existence
No disc
0F The unit lockes until the shipping switch.
12 Power OFF
OPEN key
00 Initializing
03 Carry up until the TOP switch.
04 Timer set
Repeat O/C
05 7-to-3 pulse drive.
09 Decelerated after full driving for 0.8ses.
Time out : 5sec. To LOAD
0E Play close discrimination.
Close
Lock
Unlock for 1.9sec.
PLAY key
0D Waits focus is locked. (1.9sec.)
0C Start the disc sense. LD ON
0B Move the slider to disc sense position.
0A Waits for release the slider shipping.
08 Waits until door is closed.
09 Down the carry to the BTM.
Time out : 5sec. To OPEN
Close
07 Up the carry to the top position.
Open
06 Down the carry to the MID and then check the door.
05 Waits for spindle is stopped. (Backup)
Time out : 5sec. To OPEN
02 7-to-3 pulse loading.
03 Decelerated after full loading for 0.8sec.
Time out : 5sec. To OPEN
Repeat O/C
01 After waite the time, set the timer.
00 Initializing
0A Waiting
CLOSE PLAY key

Loading signal





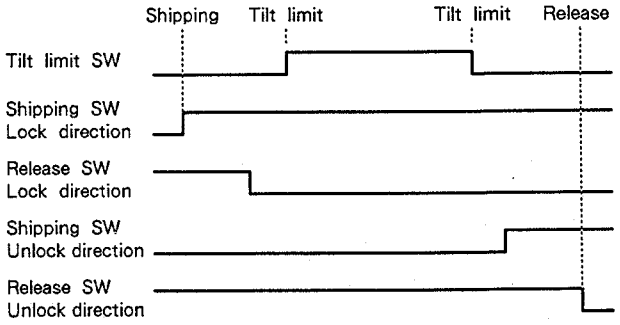
UP/DOWN counter initialization
Slider position control

RV MODE	STEP
00	Direction (REV), speed, timer set
01	Moves the slider in the REV direction until the counter value stops changing. Judges that it reaches the inner track when the value remains the same for 1 second.
02	Slider STOP, U/D counter, ϕ clear
03	Waits for 0.1 seconds.
04	Moves the slider to the disc sense position.
05	Position check (backup) Moves the slider to the disc sense position if moved.

Slider lock · Release control

LKMODE

00	Shipping switch discrimination.
01	Lock until the shipping switch is "L".
02	Waiting for the time.
03	Unlock until the limit switch is "H".
04	Measure the unlock time until the limit switch is "L".
05	Unlock until the release switch is "L".
06	Wainting for the time.
10	Lock until the limit switch is "H".
11	Lock to the tilt center. 1/2 the time obtained by measuring in 04.
12	STOP
1A	Lock until the shipping switch is "L".



11. SPECIFICATIONS

1. General

System ..... LaserVision Disc system
Laser ..... Semiconductor laser wavelength 780 nm
Power requirements ..... AC 120 V, 60 Hz
Power consumption 67W
Weight ..... 28 kg (61 lbs 11 oz)
Dimensions ..... 457 (W) x 458 (D) x 182 (H) mm
18 (W) x 18-1/16 (D) x 7-3/16 (H) in
Operating temperature ..... +5°C ~ +35°C
(41°F ~ 95°F)
Operating humidity ..... 5% ~ 90%
(There should be no condensation of moisture.)

2. Disc

LaserVision Discs

*Maximum playing times
12-inch standard play disc ..... 1 hour/both sides
12-inch extended play disc ..... 2 hours/both sides
8-inch standard play disc ..... 28 min/both sides
14 min/one side
8-inch extended play disc ..... 40 min/both sides
20 min/one side

Spindle motor speed
Standard play disc ..... 1,800 rpm
Extended play disc ..... 1,800 rpm (inner circumference)
to 600 rpm (outer circumference)
(For a 12-inch disc)

** Actual playback time differs for each disc.*

3. Video characteristics (2 pairs)

Format ..... NTSC specifications
Video output
Level ..... 1 Vp-p nominal, sync. negative, terminated
Impedance ..... 75 Ω unbalanced
Jacks ..... RCA jack/BNC jack

4. S-Video output (2 pairs)

Y (luminance) - Output level ..... 1 Vp-p (75 Ω)
C (color) - Output level ..... 286 mVp-p (75 Ω)
Jacks ..... S-VIDEO jacks

5. Audio characteristics (2 pairs)

Output level
During analog audio output ..... 200 mVrms
(1 kHz, 40%)
During digital audio output ..... 220 mVrms
(1 kHz, –20 dB)
Jacks ..... Both RCA jacks
Number of channels 2

Digital Audio Characteristics

Frequency response	4 Hz ~ 20 kHz (±0.2dB) (EIAJ)
SN ratio	115 dB (EIAJ)
Dynamic range	100 dB (EIAJ)
Channel separation	110 dB(EIAJ)
Total harmonic distortion	0.0015% (EIAJ)
Wow and flutter	Limit of measurement (0.001% W. PEAK) or less (EIAJ)

6. Other Terminals

Control input/output ..... Both miniature jacks
Optical digital output ..... Optical digital jack

7. Accessories

Remote control unit (CU-LD019) 1
Size "AA" (IEC R6) dry cell batteries 2
Video cord 1
Audio cord 1
BNC - pin plug adaptor 1
S video cord 1
Operating instructions 1

8. Player Functions

- Display ON/OFF
- Power ON/OFF by remote control unit POWER
- Picture adjustment
- Last Memory

9. Functions

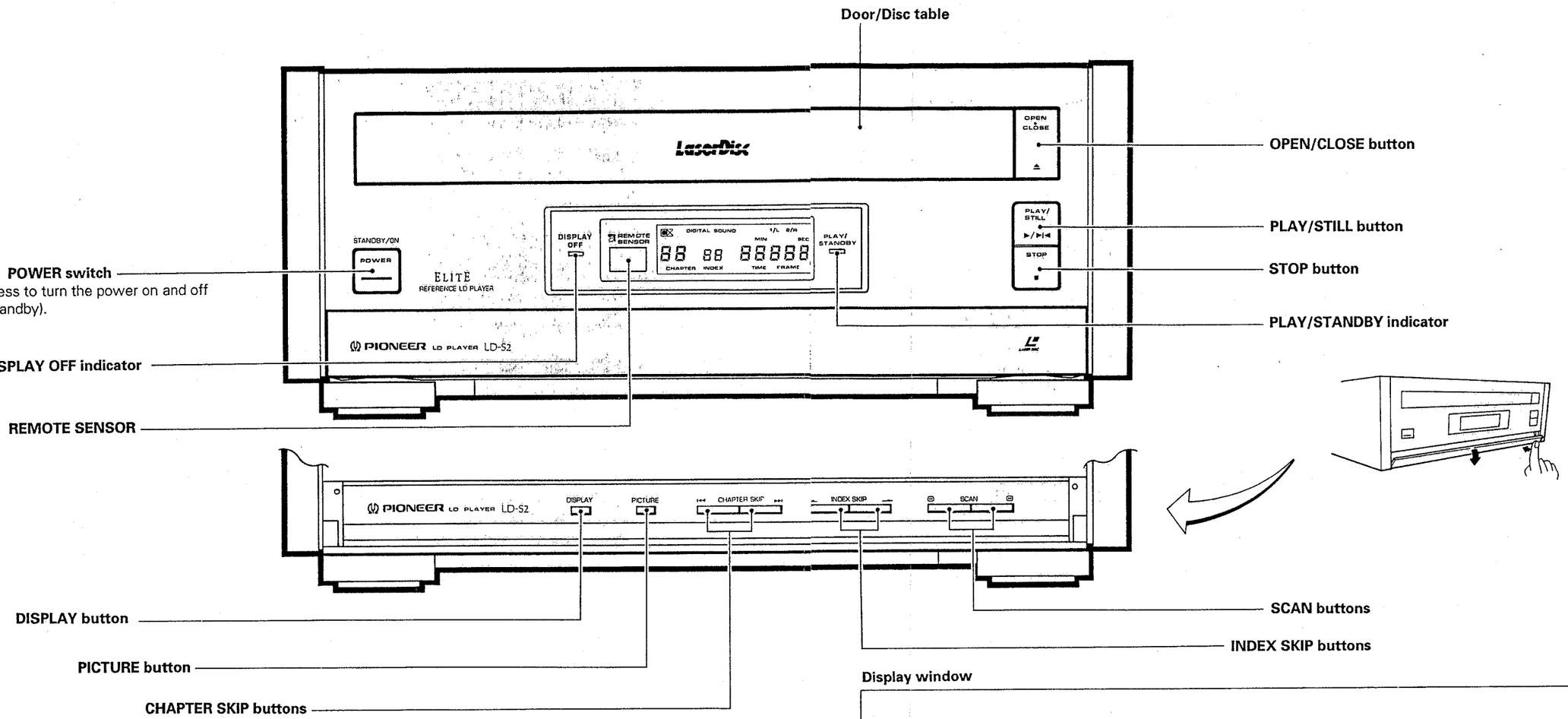
Remote control unit operations (CU-LD019)

	Function	Standard play Disc (CAV)	Extended play Disc (CLV)
Basic Functions	Single-side play	YES	YES
	Pause	YES	YES
	Stop	YES	YES
Search	Fast forward and reverse	YES	YES
	Chapter skip	YES	YES
	Index skip	YES*1	YES*1
	Direct chapter number search	YES	YES
	Frame number search	YES	NO
	Time number search	NO	YES
Program	Chapter program play	YES	YES
	Program correction	YES	YES
Repeat	Repeat between 2 points	YES	YES
	Memory repeat	YES	YES
	Chapter repeat	YES	YES
	One-side repeat	YES	YES
	Program repeat	YES	YES
Trick play	Still/Step (Forward/Reverse)	YES	YES
	Multi-speed (Forward/Reverse 9-level variable)	YES	YES
	Still with Sound	YES	YES
	Strobe motion	YES	YES
	Jog dial/Shuttle ring	YES	YES
Time display	Elapsed time display	YES*1	YES*1
	Remaining total time display	YES*1	YES*1
	Total number of chapters, total time display	YES*1	YES*1
Others	CX system ON/OFF	YES*2	YES*2
	AUTO DIGITAL/ANALOG switch	YES*3	YES*3
	One-shot memory	YES	YES
	Audio channel selection (Stereo, 1/L, 2/R)	YES	YES
	Last memory	YES	YES

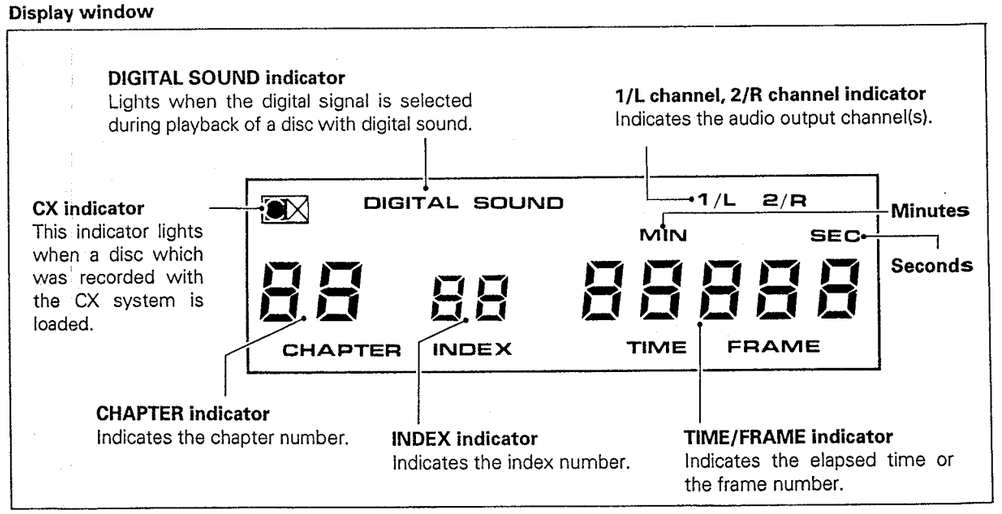
*1 Only discs with TOC
*2 Valid for analog sound playing a disc with the CX mark.
*3 Can only be used with discs with digital sound tracks.

NOTE:
The specifications and design of this product are subject to change without notice, due to improvement.

12. PANEL FACILITIES



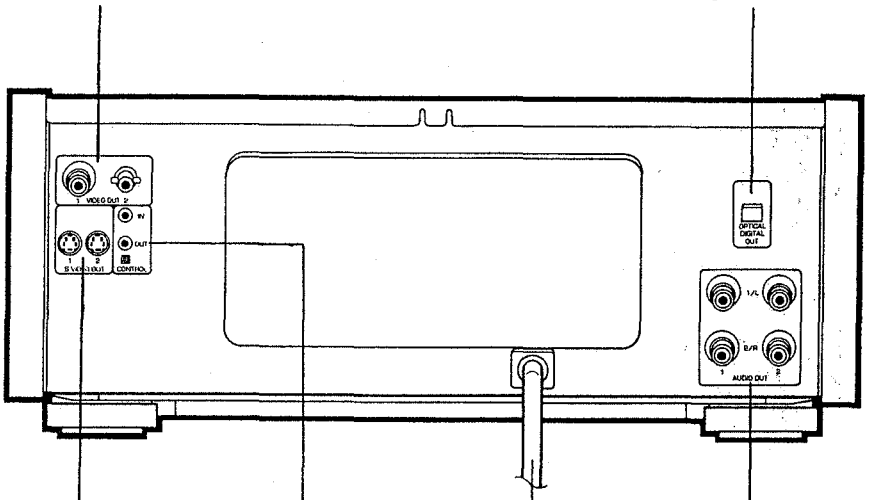
Display window



VIDEO OUT 1/2 jacks
Connect to the Video Input jack of the TV.

1 **(RCA jack):** When this jack is connected to the Video Input jack of the TV, the information regarding the operations can be displayed on the monitor TV screen.
2 **(BNC-pin plug adapter jack):** When this jack is connected to the Video Input jack of the TV, only the video signal is output and the information display cannot be carried out.

OPTICAL DIGITAL OUT jack
This jack outputs the optical digital signals of the audio data and subcode (signals which can be recorded together with the audio signal).



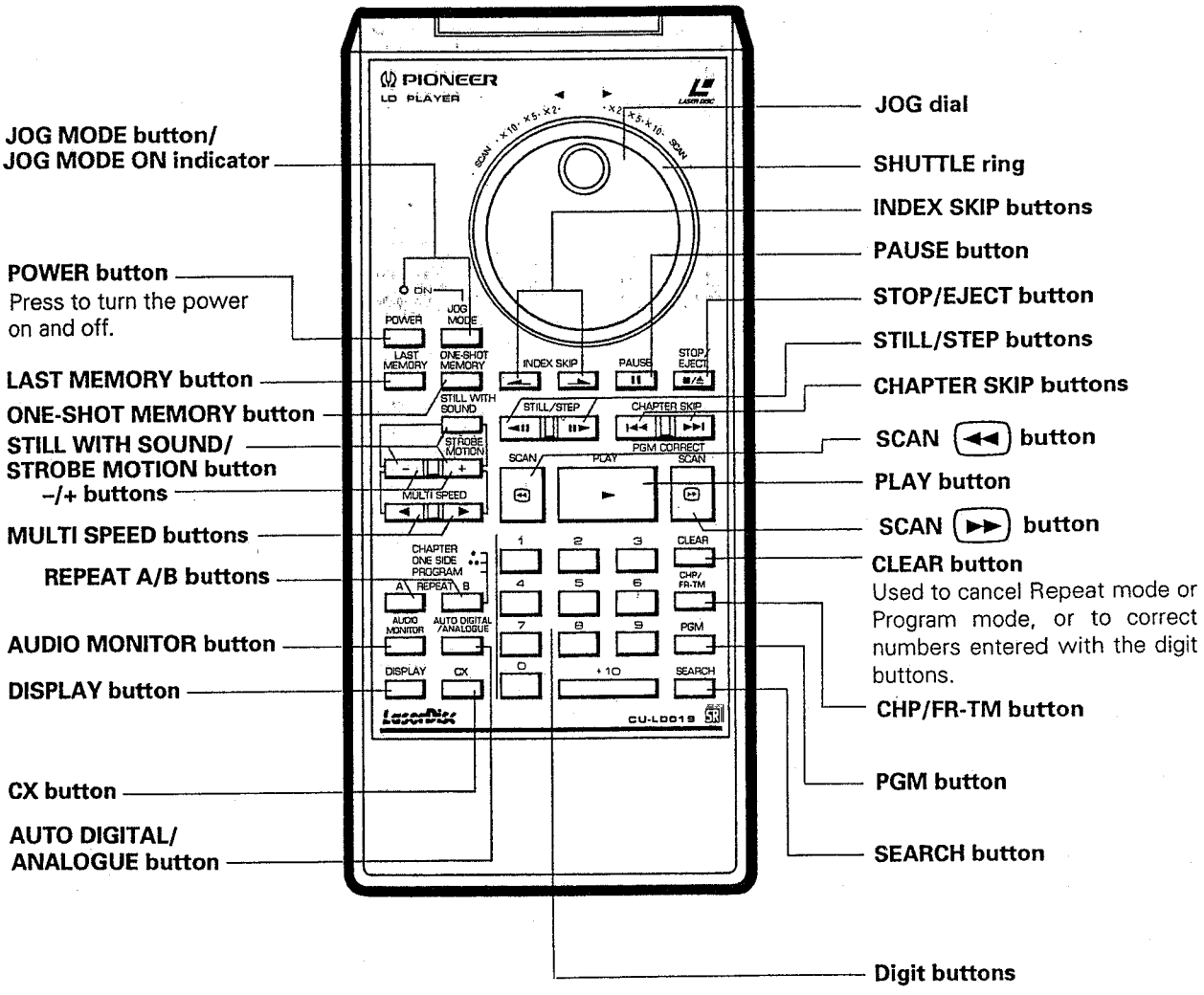
S VIDEO OUT jacks
Connect to the S Video Input jack of the TV.

1: When this jack is connected to the S Video Input jack of the TV, the information regarding the operations can be displayed on the TV screen and display window of the player.
2: When this jack is connected to the S Video Input jack of the TV, only the video signal is output and the information display cannot be carried out.

AUDIO OUT jacks
Connect to the CD or VDP Audio Input jacks of the stereo amplifier. Never connect to the *PHONO* jacks.

CONTROL IN/OUT jacks
System control can be performed when these jacks are connected to a product that has the SR mark.

Power cord
Connect to an AC wall outlet.

When the power cord of this player is connected to an AC outlet, power is supplied to the player's internal memory (such as the last memory) even when the POWER switch is STANDBY. Therefore, be sure to connect the power cord directly to a wall outlet. If the power cord is connected to an outlet such as a switched outlet on an amplifier, the memory contents will be erased whenever the amplifier's power switch is turned off.

Remote control buttons with the same names or marks as buttons on the front panel of the player control the same operations as the corresponding front panel buttons.